Welcome To

ISSCC 2014
SESSION 7

Image Sensors

A 1/4-inch 8Mpixel CMOS Image Sensor with 3D Backside-Illuminated 1.12μm Pixel with Front-side Deep-Trench Isolation and Vertical Transfer Gate

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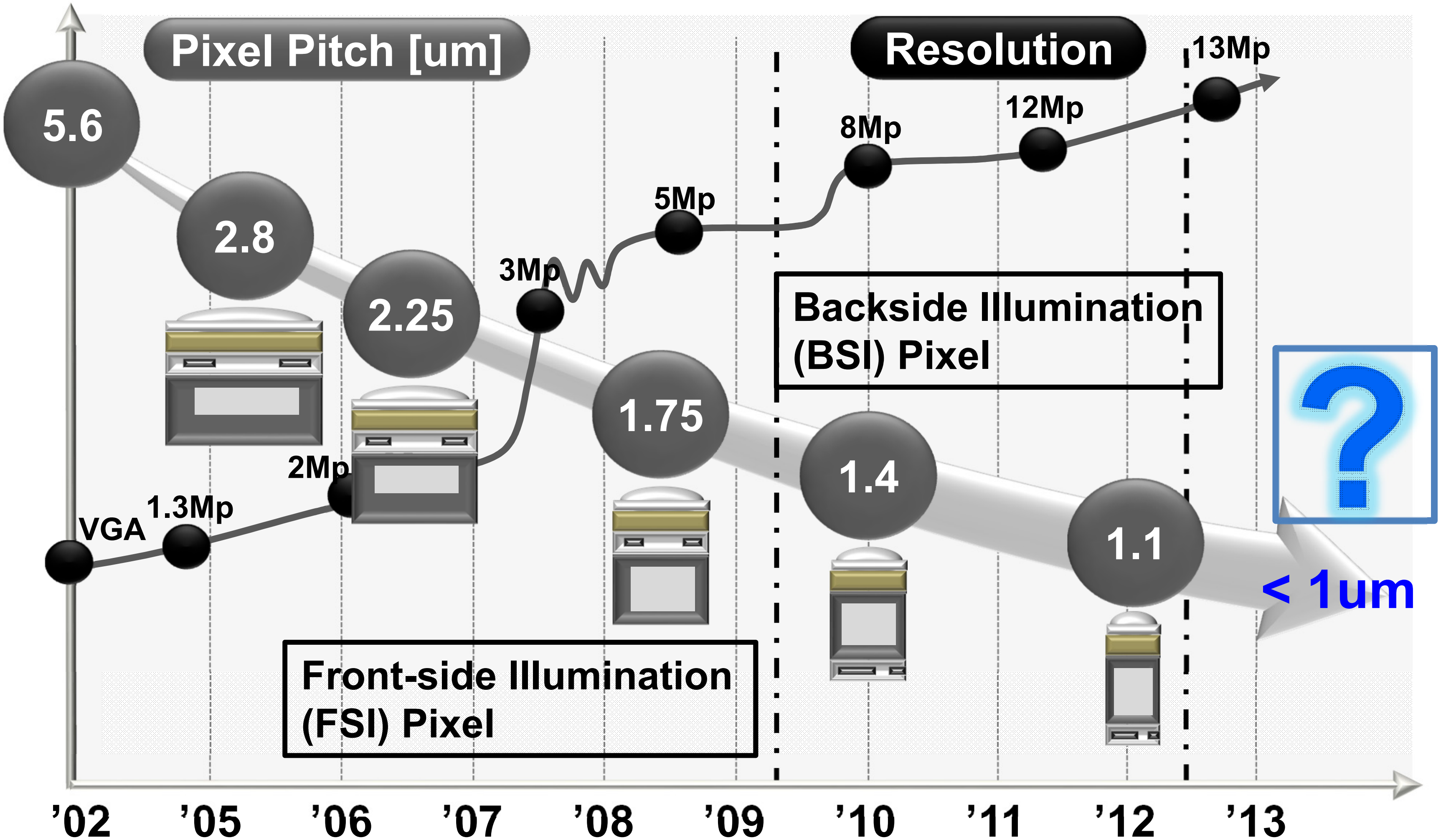
Samsung Electronics, Yongin, Korea

Outline

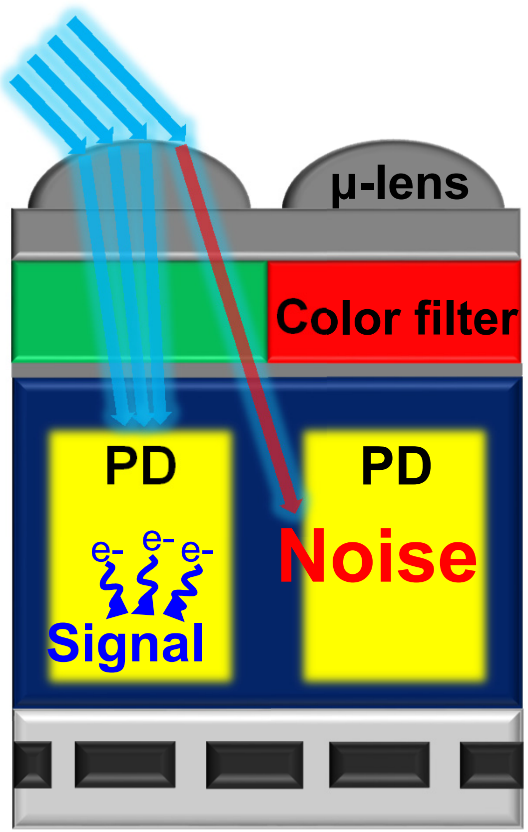
- Background
- Next Pixel Structure after BSI
- New Pixel with
  Front-side Deep Trench Isolation(F-DTI)
  AND
  Vertical Transfer Gate(VTG)
- Experimental Results
- Summary

High Resolution Trend and Pixel Shrinkage



SNR at Low-light Condition

- Signal is determined by **sensitivity**
- Noise is governed by photon shot noise, dark noise, and **crosstalk**

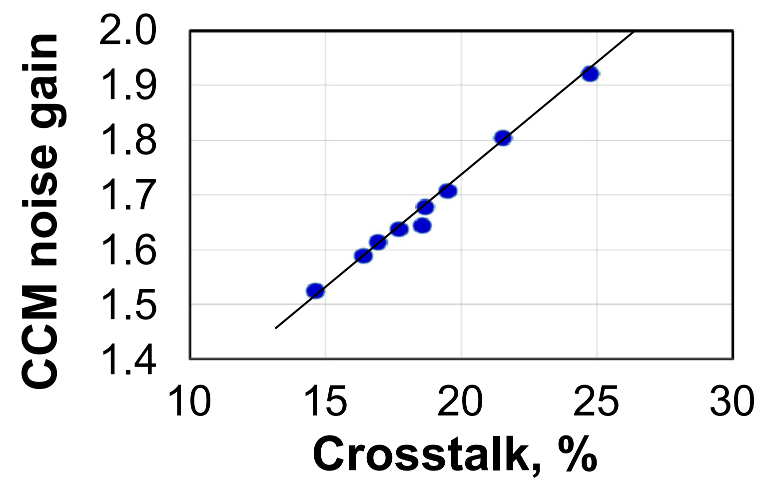


$$\frac{S}{N}$$

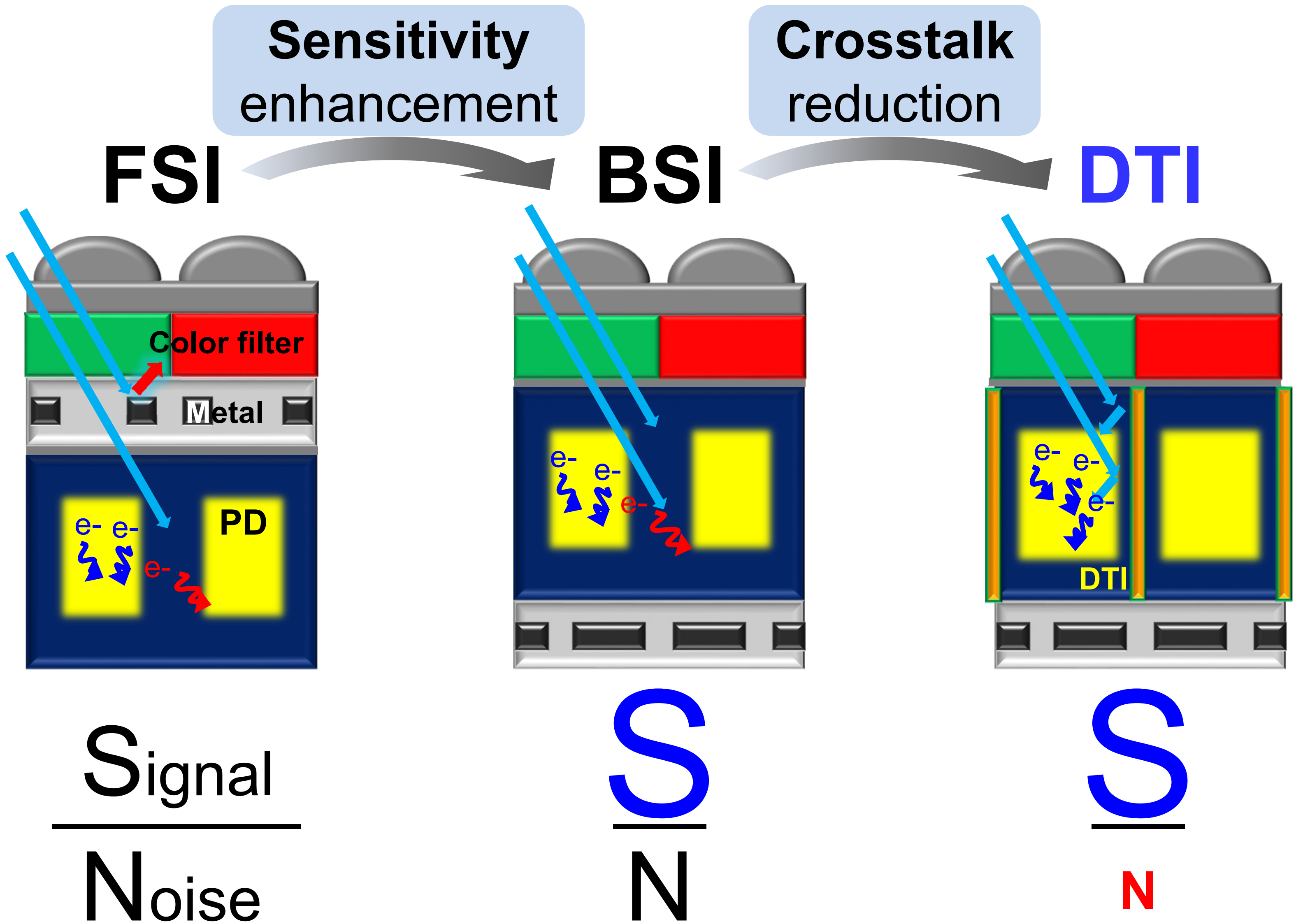
Color Correction Matrix (CCM) noise gain

$$\begin{pmatrix}R'\\G'\\B'\end{pmatrix} = \begin{pmatrix} D_R & \alpha & \beta \\ \gamma & D_G & \delta \\ \varepsilon & \varphi & D_B\end{pmatrix}\begin{pmatrix}R\\G\\B\end{pmatrix}$$

$$: \frac{\sqrt{C_R^{\,2}(D_R^{\,2}+\alpha^2+\beta^2)+C_G^{\,2}(\gamma^2+D_G^{\,2}+\delta^2)+C_B^{\,2}(\varepsilon^2+\varphi^2+D_B^{\,2})}}{\sqrt{C_R^{\,2}+C_B^{\,2}+C_G^{\,2}}}$$

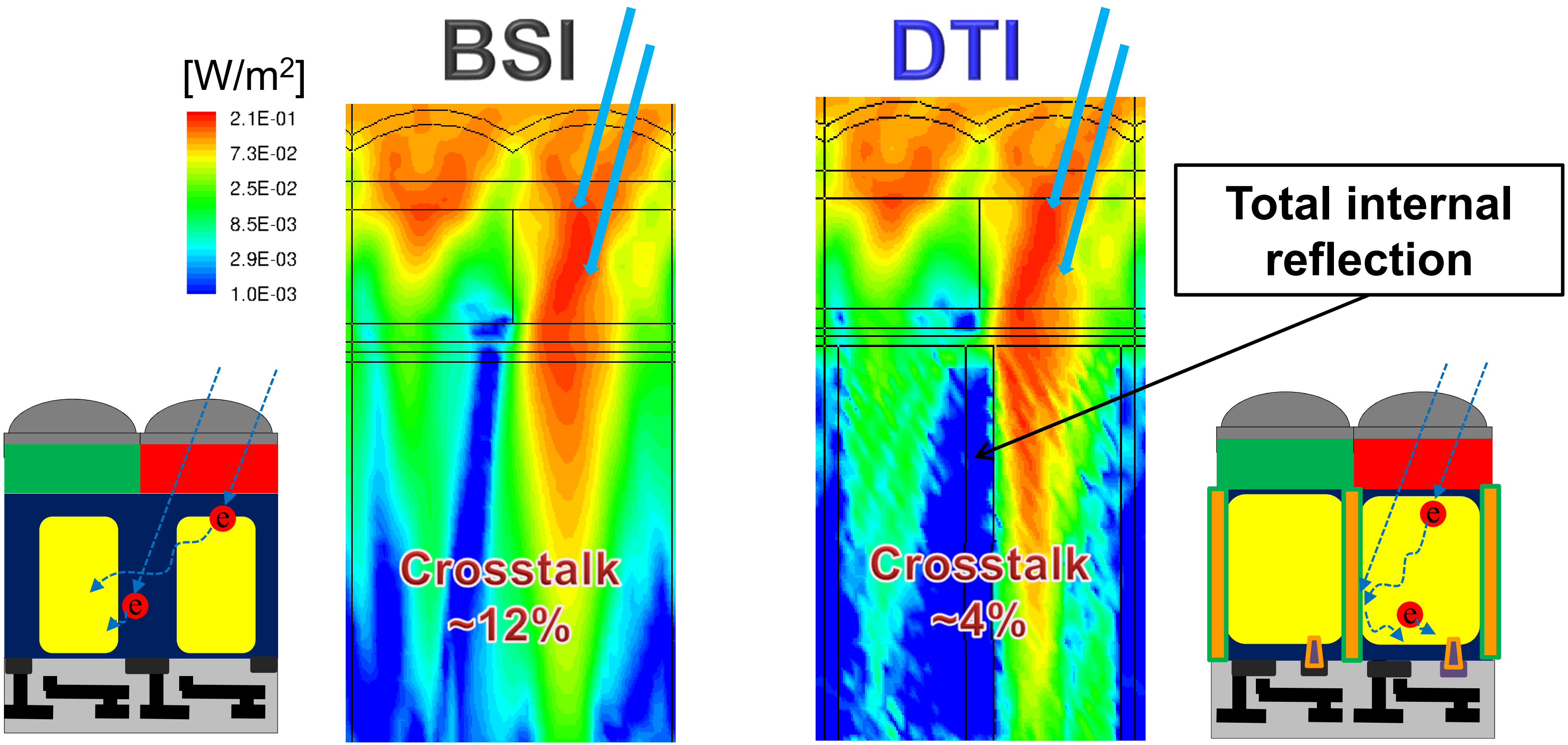


How to Enhance SNR



Crosstalk Simulation

- DTI-introduced physical isolation prevents both optical and electrical crosstalk between pixels

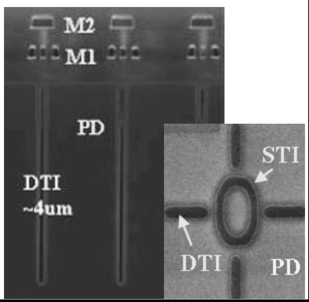
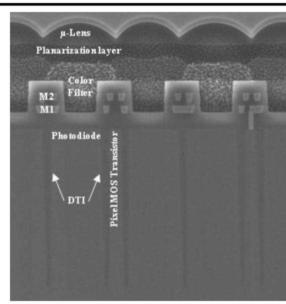
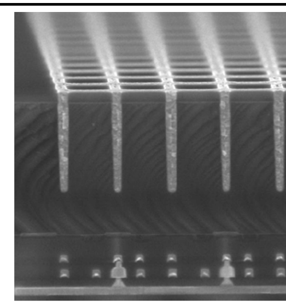


*Crosstalk, from red to green, except color filter crosstalk.

Previous Works for DTI Pixel

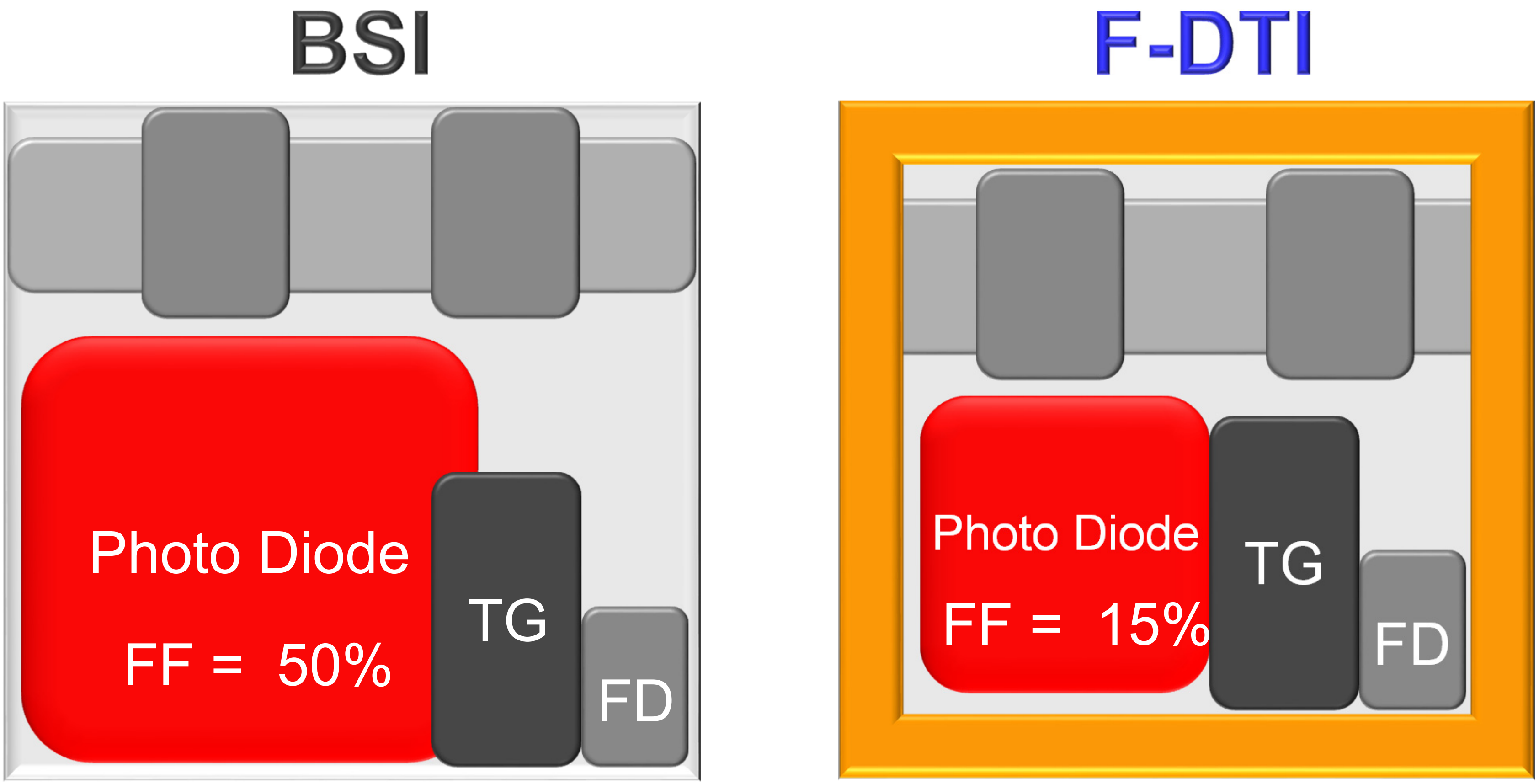
- F-DTI with *full depth* and *full surrounding* in the *smallest pixel(~1um)* has not yet reported

Front-side DTI (F-DTI), Back-side DTI(B-DTI)

	JJAP'07, Samsung	IISW '11, STM	IEDM '12, Toshiba	IISW '13, Chipworks (STM)	**This work**
Structure				**No Image available**	
Features	• 1.7um-pitch	• 1.4um-pitch	• 1.12um-pitch	• 2.0um >>1.12um	• ≤ 1.12um
	•F-DTI	•F-DTI	•B-DTI	•F-DTI	•F-DTI
	•FSI	•FSI	•BSI	•BSI	•BSI
	•Not full depth	•Not full depth	•Not full depth	•Full depth	•Full depth
	•Not full surrounded	•DTI invaded inside pixel	•Full surrounded	•Full surrounded	•Full surrounded
				•Difficult to shrink to ~1.0um	•Small size pixel near ~1.0um

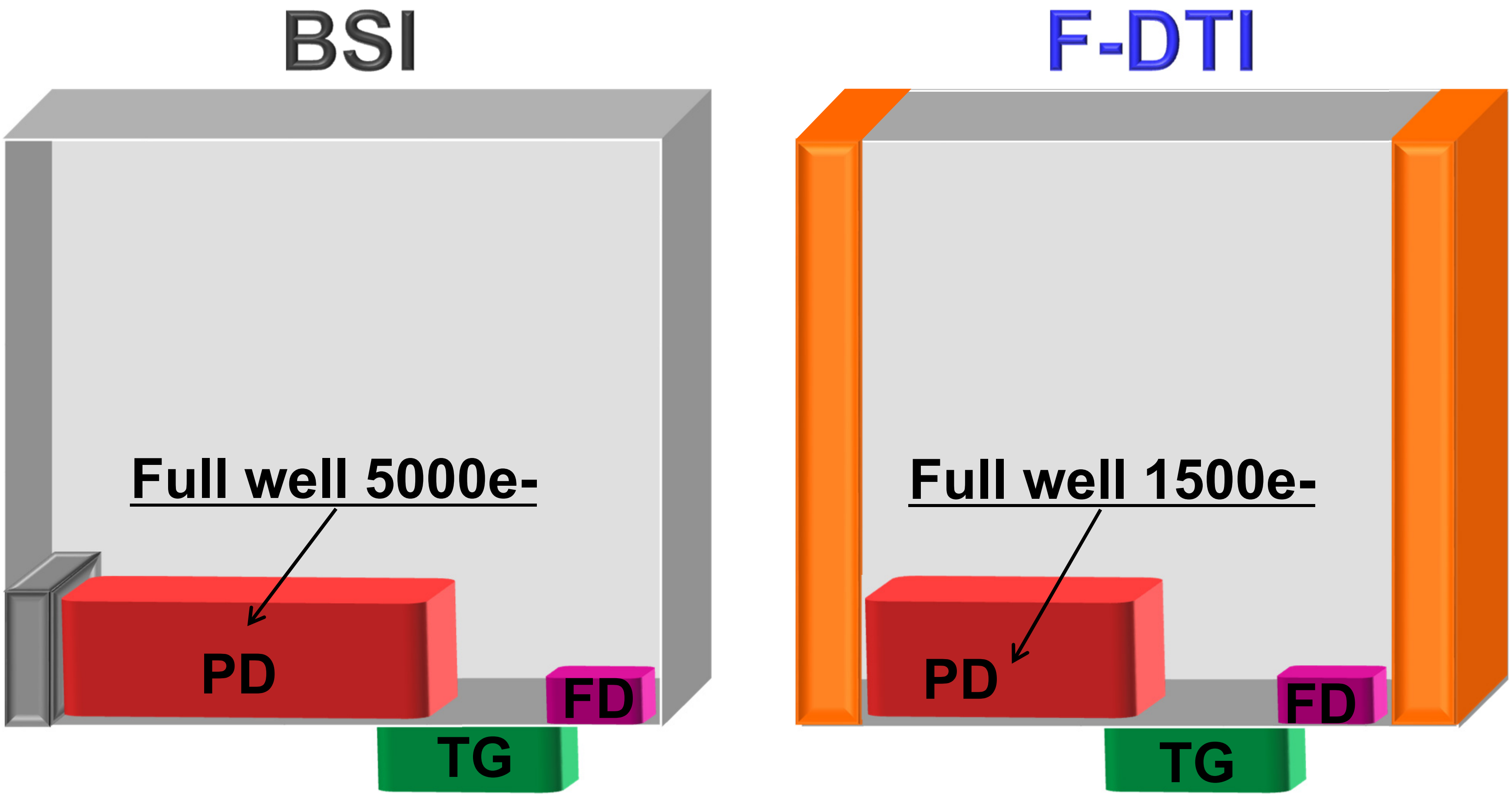
Problem by F-DTI Introduction in Small Pixel

- The effective photodiode area is reduced by the amount of DTI width → low full well capacity



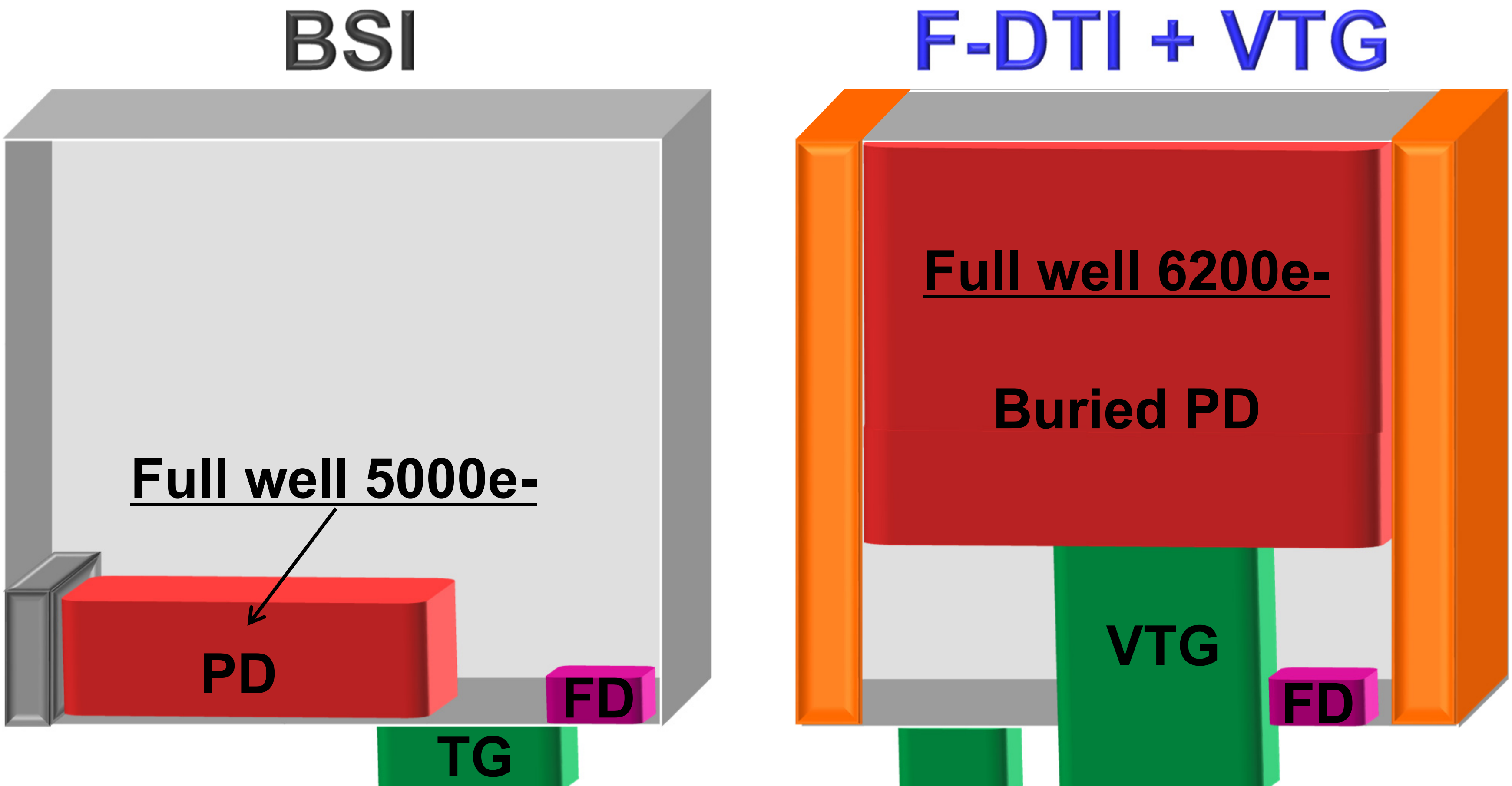
Problem by DTI Introduction in Small Pixel

- The effective photodiode area is reduced by the amount of DTI width → low full well capacity



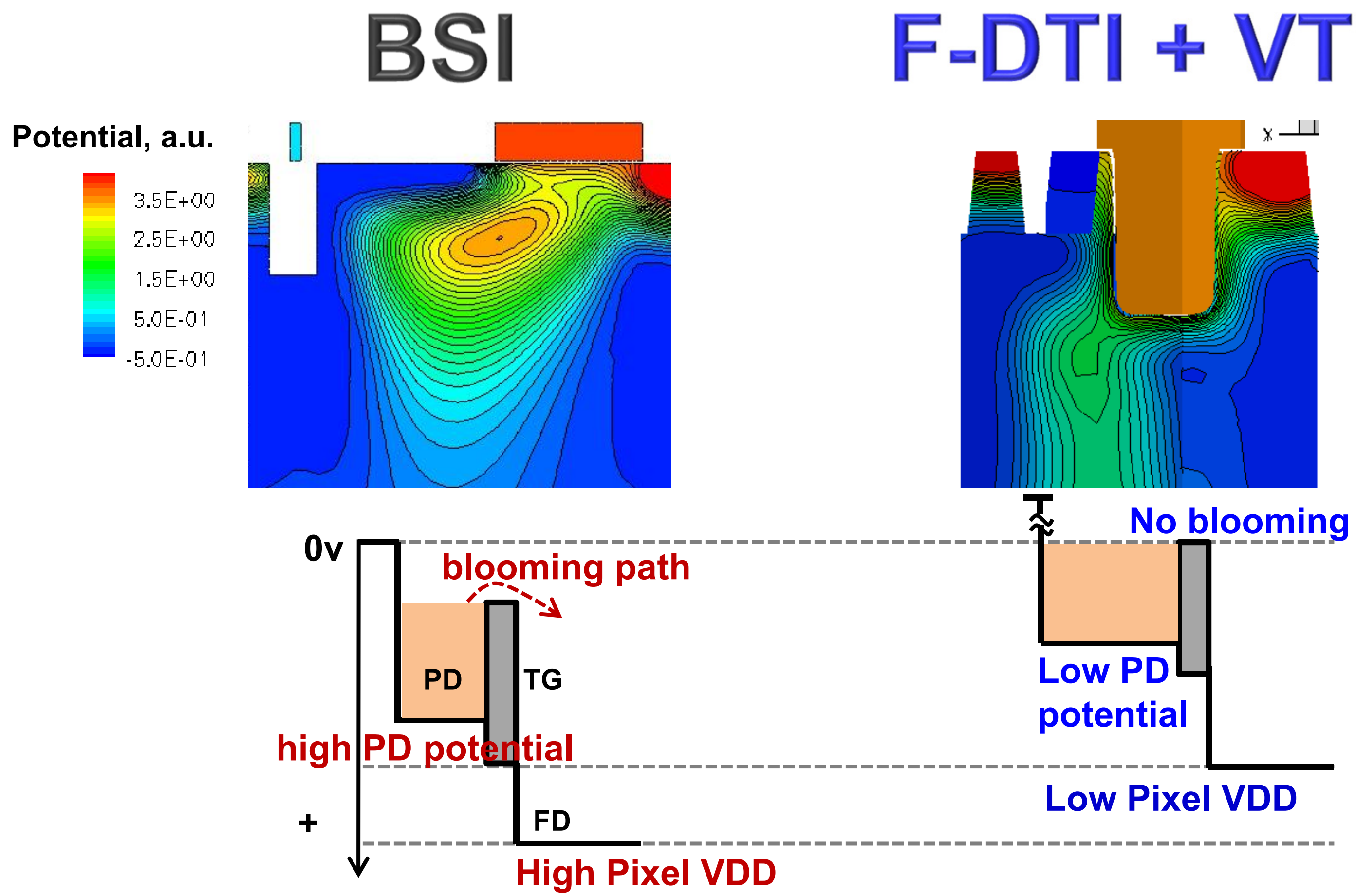
3D Pixel with VTG & Buried PD

- VTG and Buried Photodiode are introduced
  → Space of transistors and photodiodes are separated VERTICALLY



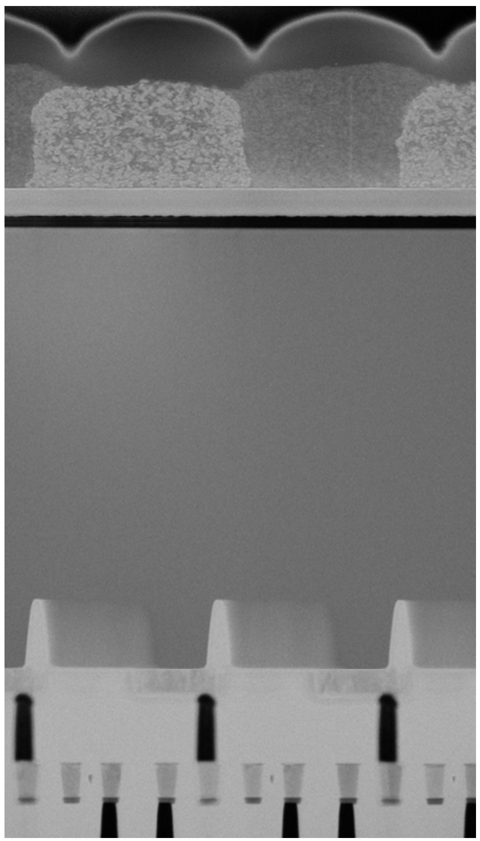
VTG Simulation

- Superior charge transfer capability of VTG and blooming free of DTI enables low-voltage operation

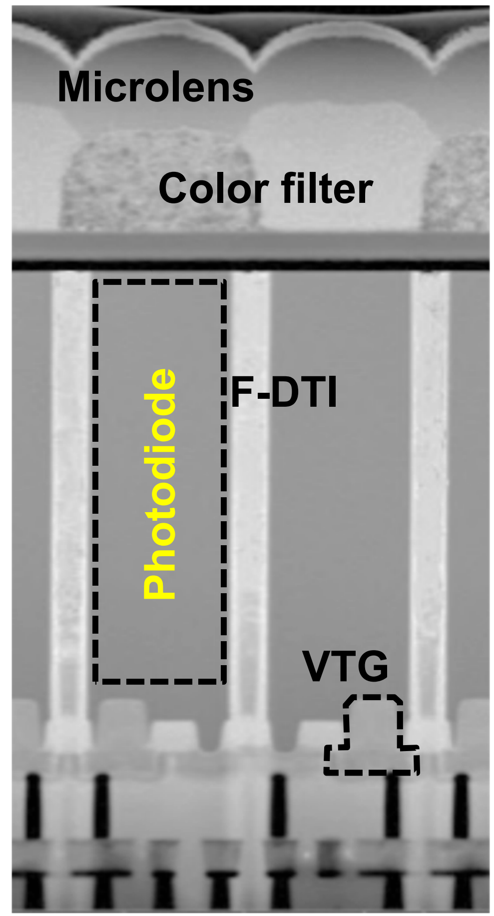


Fabricated F-DTI + VTG Pixel

BSI

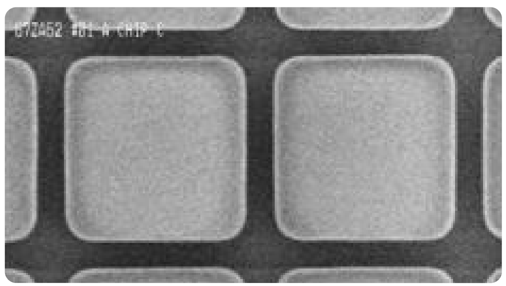


F-DTI + VTG

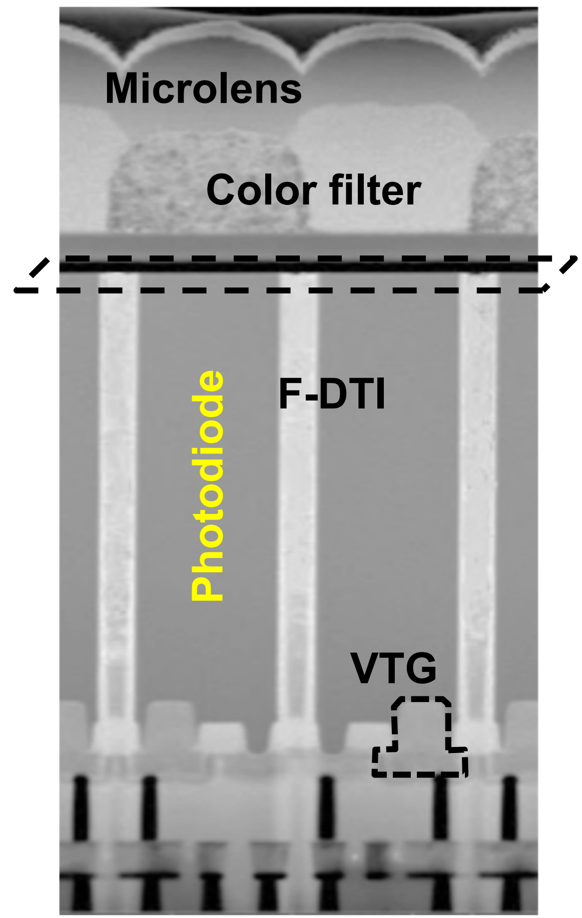


Fabricated F-DTI + VTG Pixel

Back Surface
(Fully surrounded)

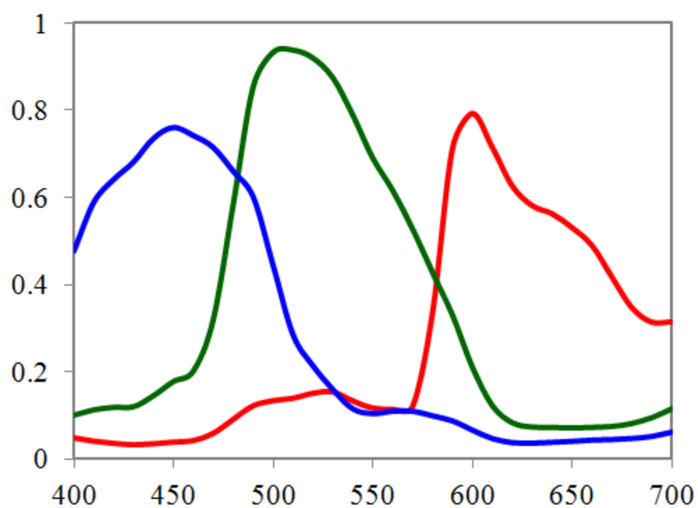
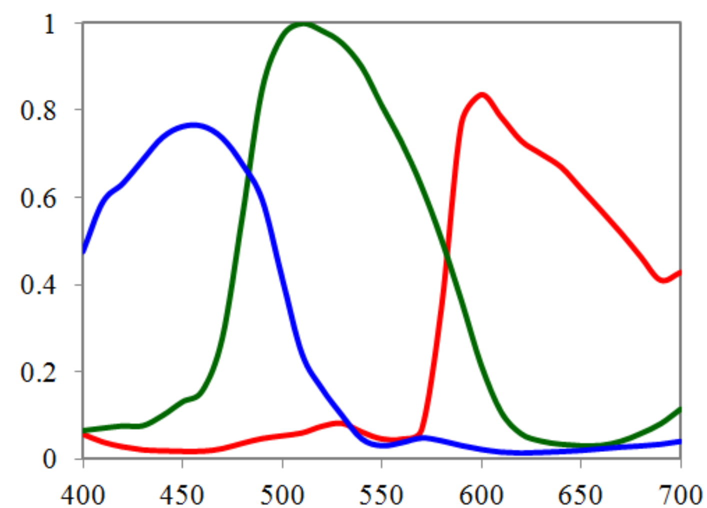


F-DTI + VTG



Quantum Efficiency Spectra

- Crosstalk: 19.0 → 12.5%
- Smaller CCM(color correction matrix) coefficients

	1.12u Conventional BSI		1.12u Front DTI + VTG
Quantum Efficiency			
Crosstalk [%]	19.0	▽35%	12.5
CCM	$\begin{bmatrix} 1.91 & -1.00 & 0.09 \\ -0.08 & 1.44 & -0.36 \\ -0.06 & -0.98 & 2.04 \end{bmatrix}$		$\begin{bmatrix} 1.58 & -0.62 & 0.04 \\ -0.03 & 1.25 & -0.22 \\ -0.03 & -0.67 & 1.70 \end{bmatrix}$

YSNR10

- YSNR10 is greatly improved: 150 → 105lux

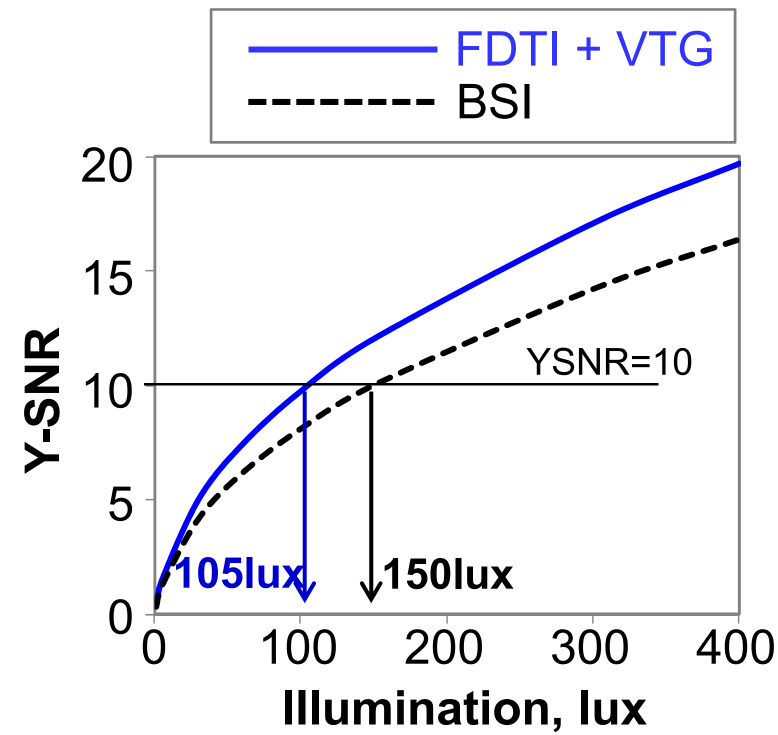
Y coefficients

$$Y=\left(0.299\ \ 0.587\ \ 0.114\right)\overbrace{\begin{pmatrix} a & b & c \\ d & e & f \\ g & h & i \end{pmatrix}}^{\text{Color Matrix}}\overbrace{\begin{pmatrix} Rgain & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & Bgain \end{pmatrix}}^{\text{WB Matrix}}\begin{pmatrix} R \\ G \\ B \end{pmatrix}$$

$$=\left(0.299\ \ 0.587\ \ 0.114\right)\begin{pmatrix} R' \\ G' \\ B' \end{pmatrix}$$

$$=0.299R'+0.587G'+0.114B'$$

CIS raw → White balance (WB) → Color correction



Reference

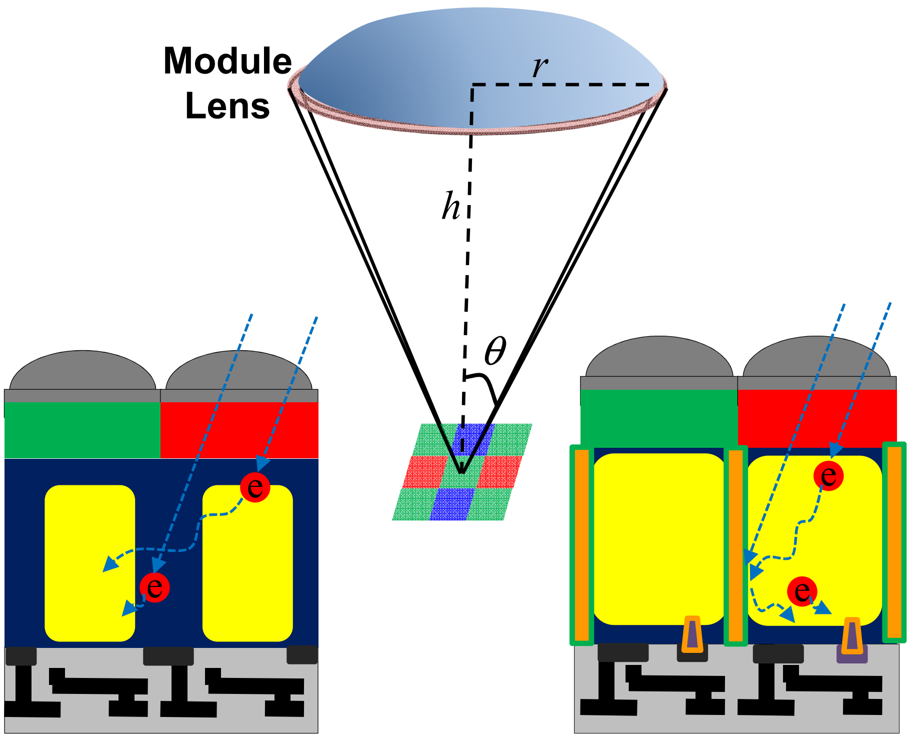
1) J. Alakarhu, *Int. Image Sensor Workshop, pp. 1-4, 2007.*

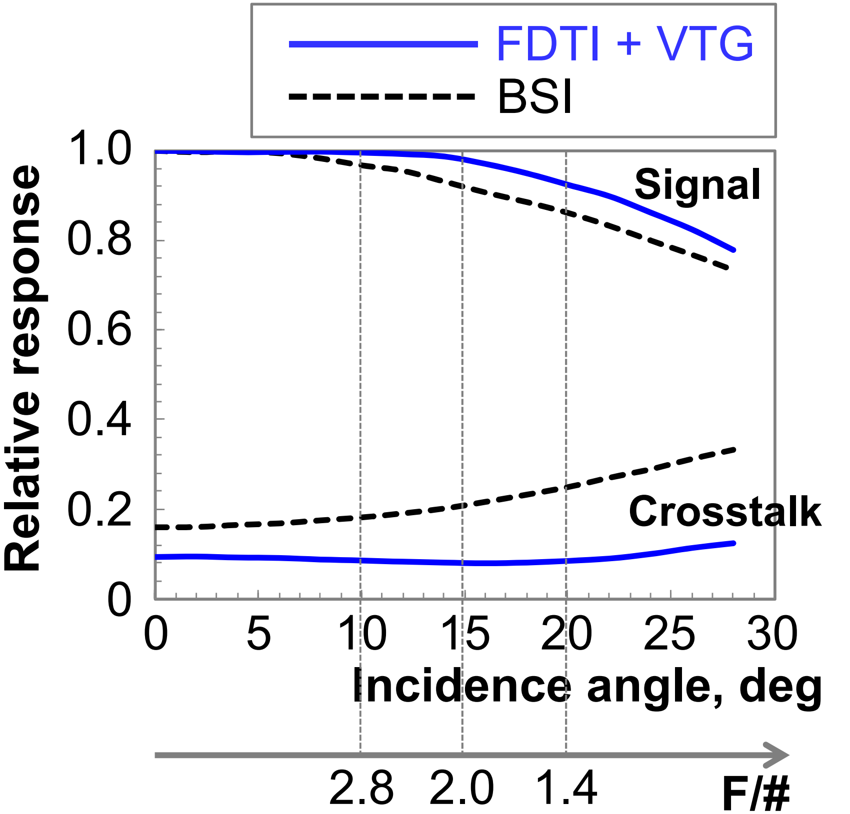
2) S. Koskinen et al, *Int. Image Sensor Workshop, pp. 114-117, 2011.*

Wider View Angle

- Better tolerance for oblique incident light of F-DTI pixel → Lower F-number lens for higher sensitivity is possible

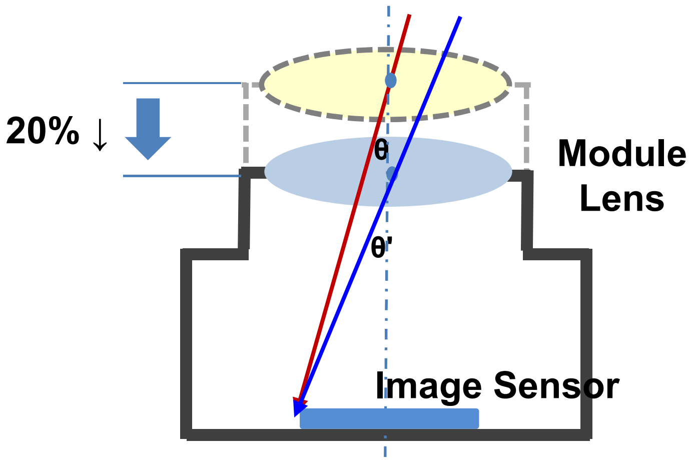
$$F = \frac{1}{NA} = \frac{h}{2r} = \frac{1}{2\tan\theta}$$

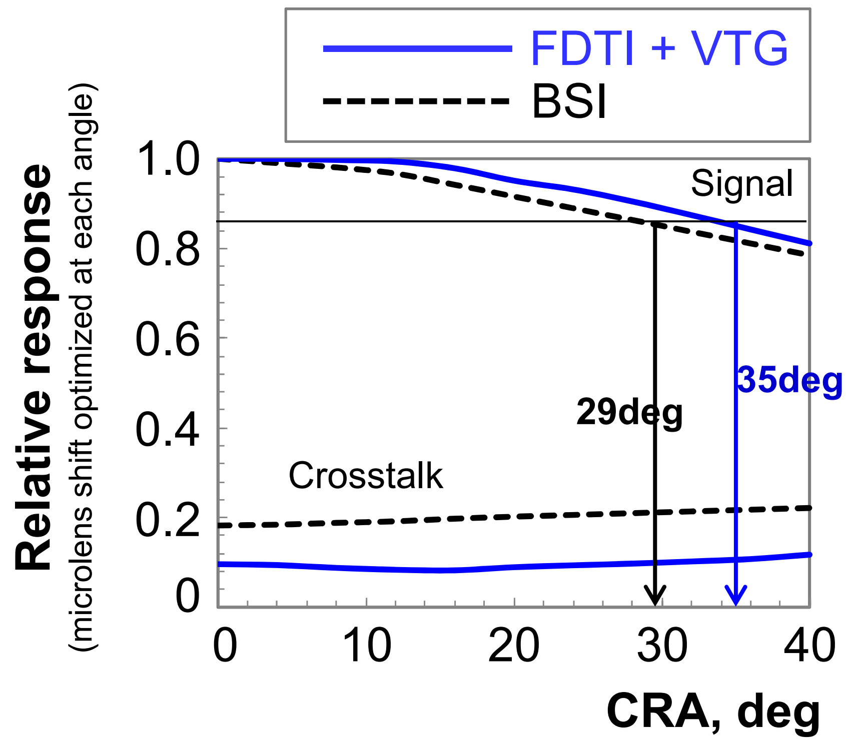




Higher Maximum CRA
(Chief Ray Angle)

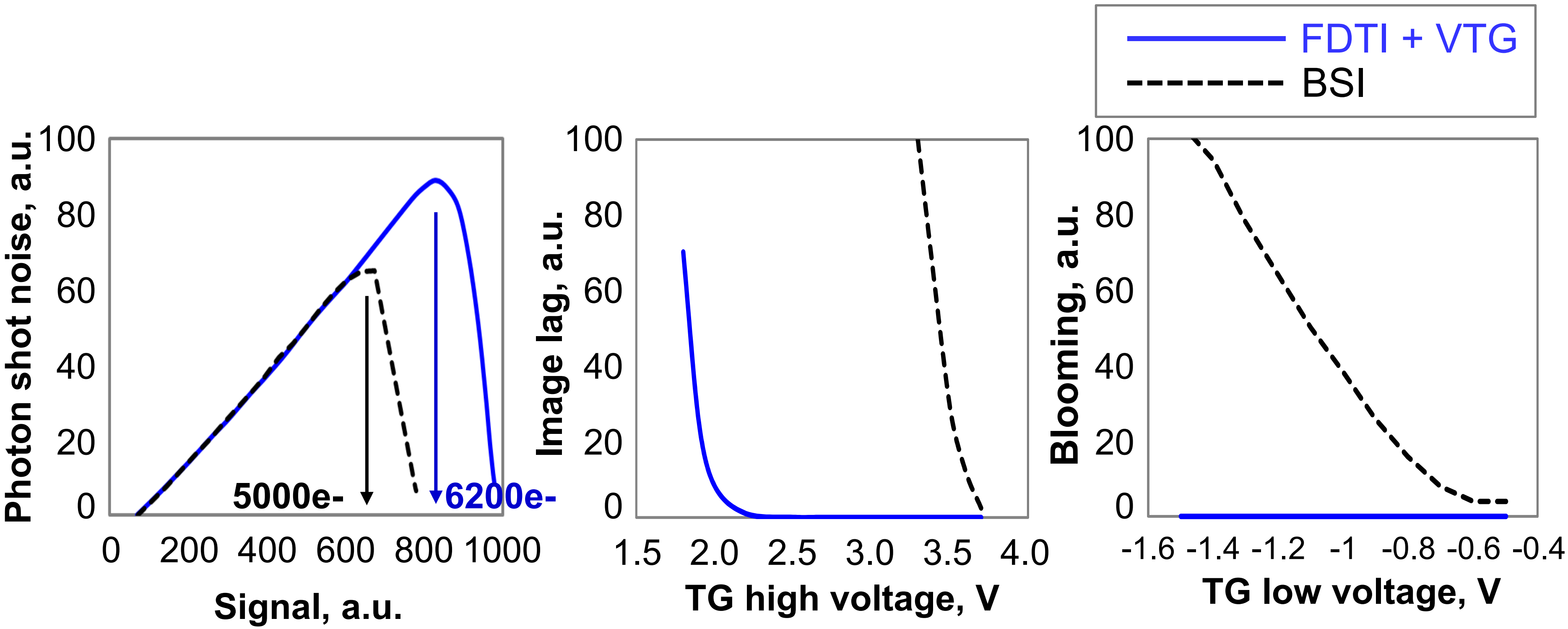
- Lower module height or larger array size allowed





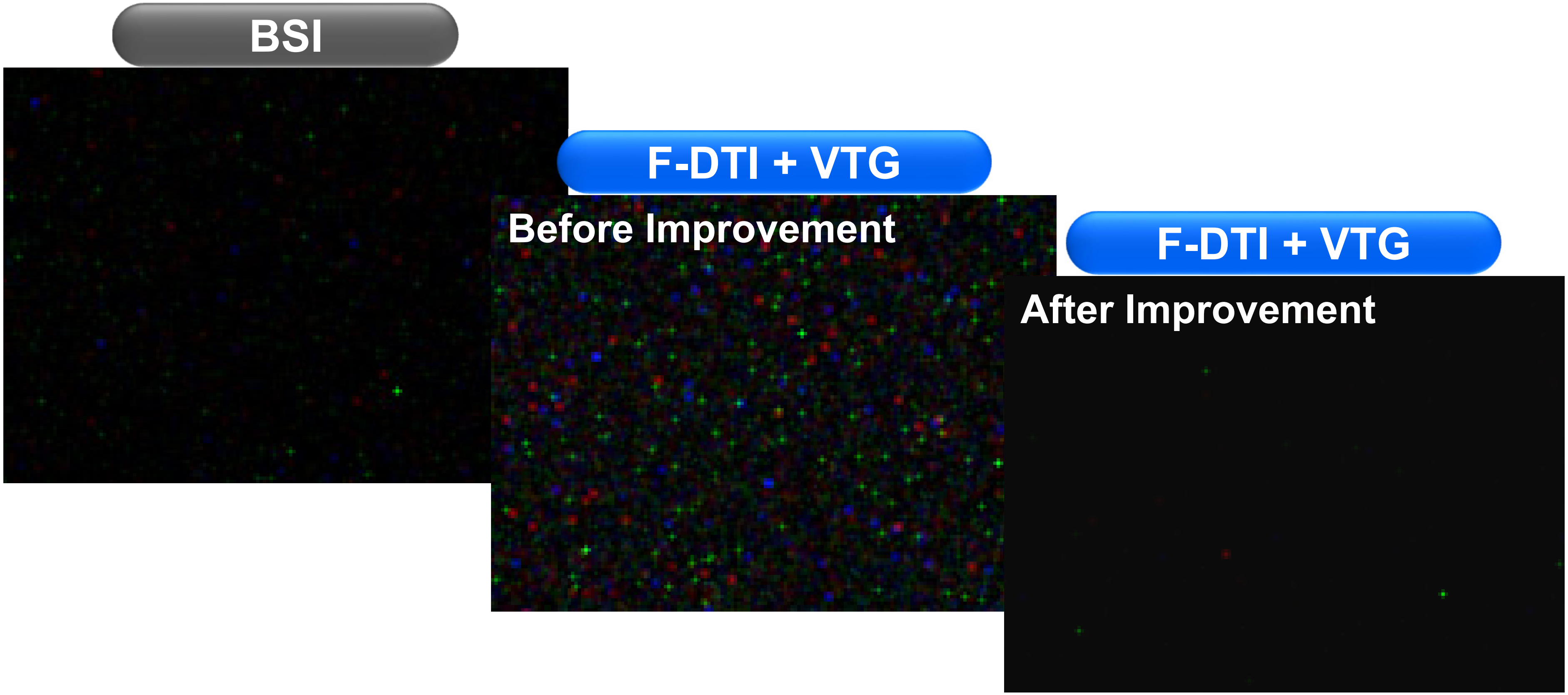
Electrical Characteristics

- 24% larger full well capacity
- Almost zero lag even @TG=2.5V
- No blooming even at highly negative TG bias



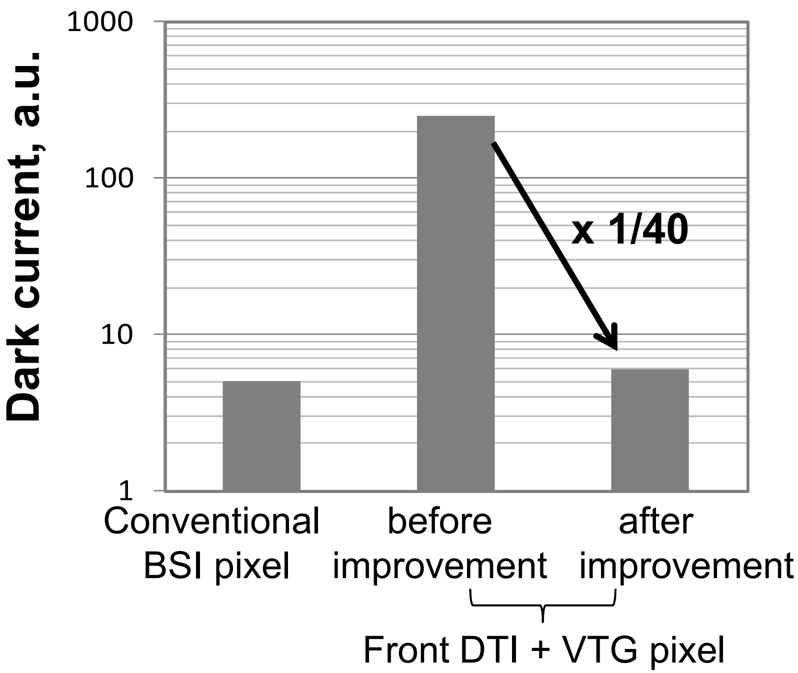
Dark Characteristics

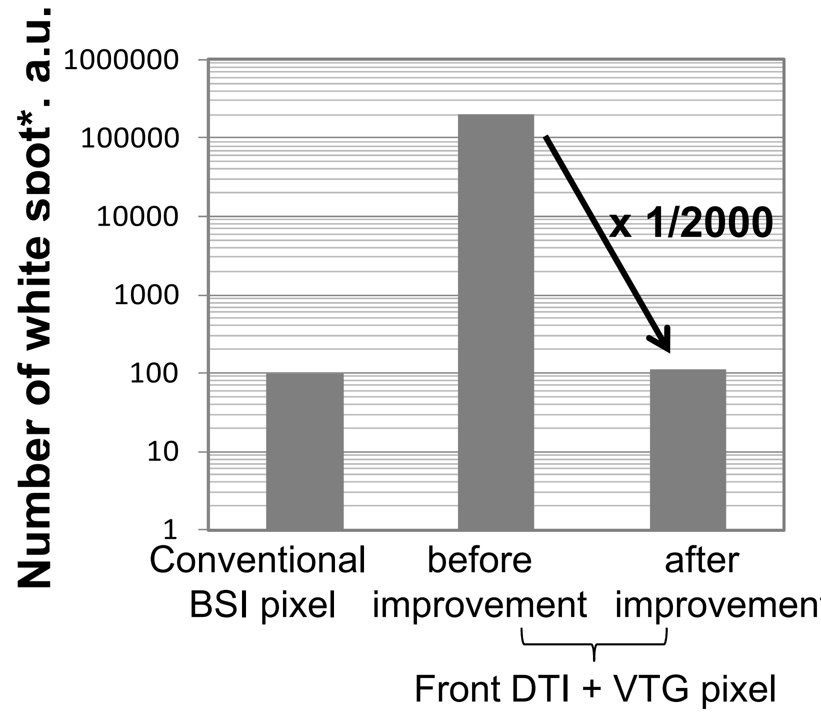
- After improving processes, overall dark characteristics(80℃) are achieved as good as conventional BSI



Dark Characteristics

- By process improvement, x1/40 dark current, x1/2000 defect counts
- Similar level to conventional BSI pixel





* White spot: # of pixels >80LSB @ gain x8, 133msec, 60℃

Performance Summary

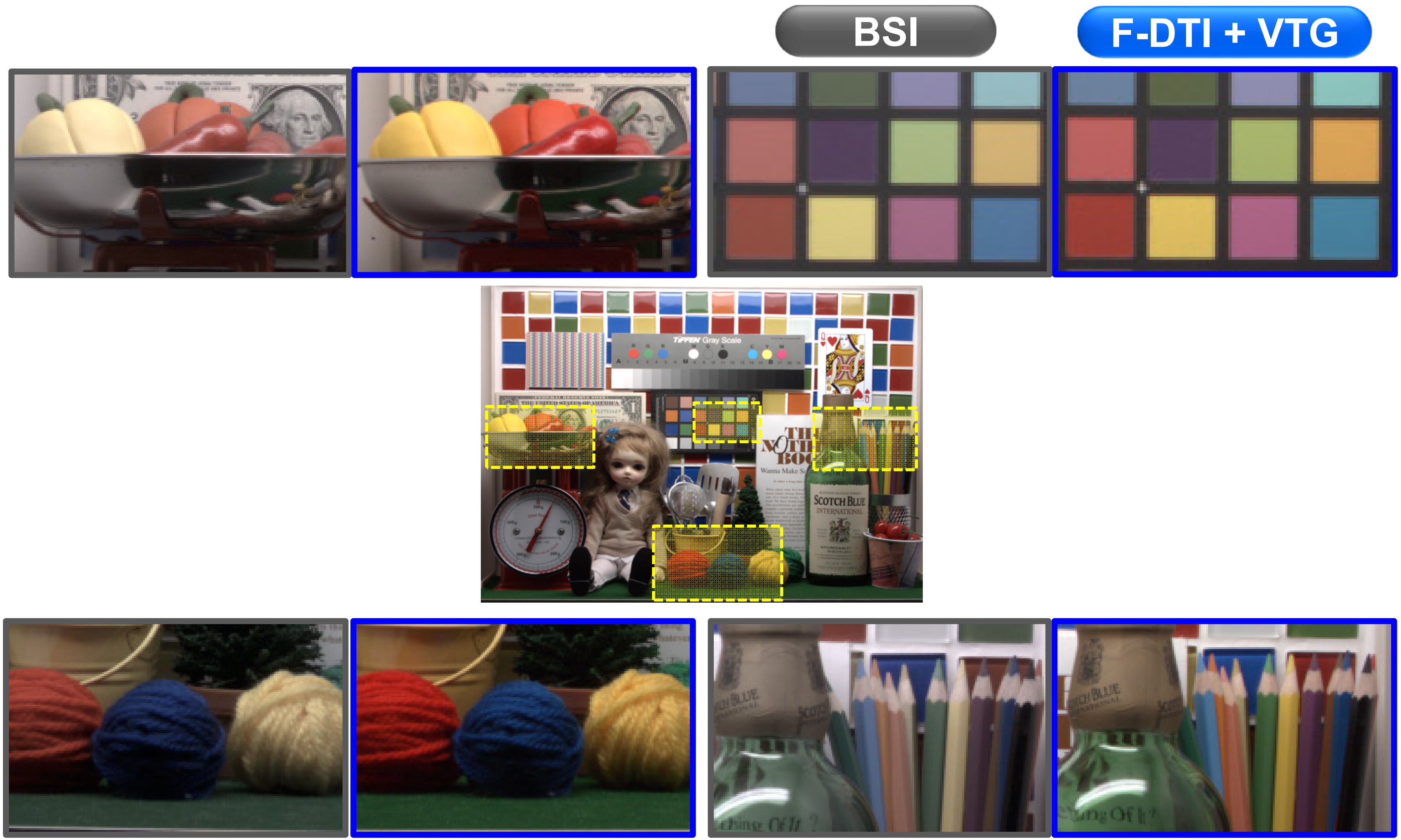
	Unit	1.12u Conventional BSI	1.12u Front DTI + VTG
YSNR10*	lux	150	105
G-Sensitivity @D65-light	e-/lux.sec	3960	4080
Crosstalk	%	19.0%	12.5%
Linear full well	e-	5,000	6,200
Dark temporal noise	e-	1.7	1.7
Dark fixed pattern noise	e-	1.0	1.0
Dynamic range	dB	68.1	69.9
Dark current @60^{o}C	e-/s	5	6
White spot**	ea/Mp	100	110

* YSNR10: illumination for Y-SNR=10
with AWB, CCM , F/2.8, 3200K-light, 18% reflectance gray patch,
80% lens transmittance, color accuracy(△E2000)=2.5

** White spot: # of pixels >80LSB @ gain x8, 133msec, 60^{o}C, dark

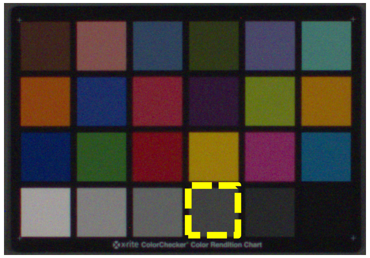
Image of 8M F-DTI + VTG CIS

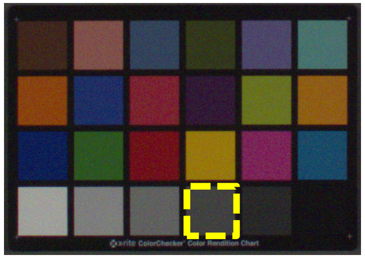
Low Crosstalk, w/o CCM

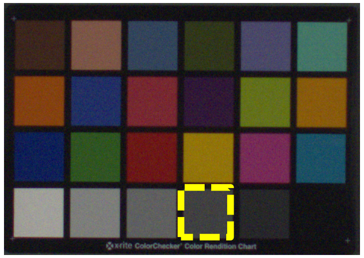


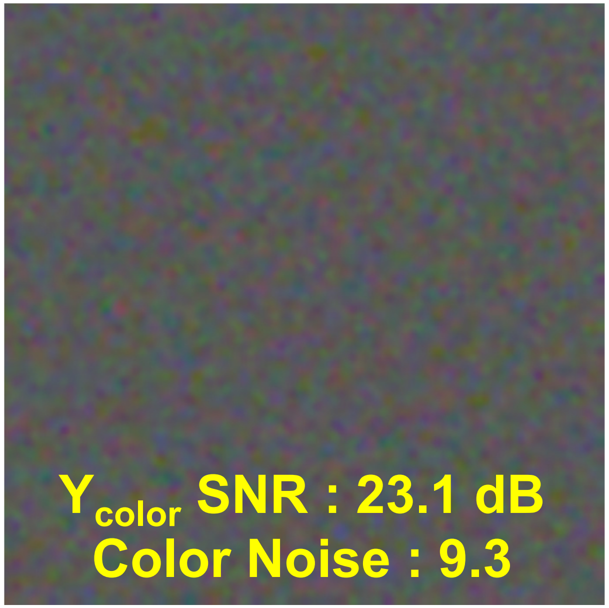
Low Crosstalk → High SNR

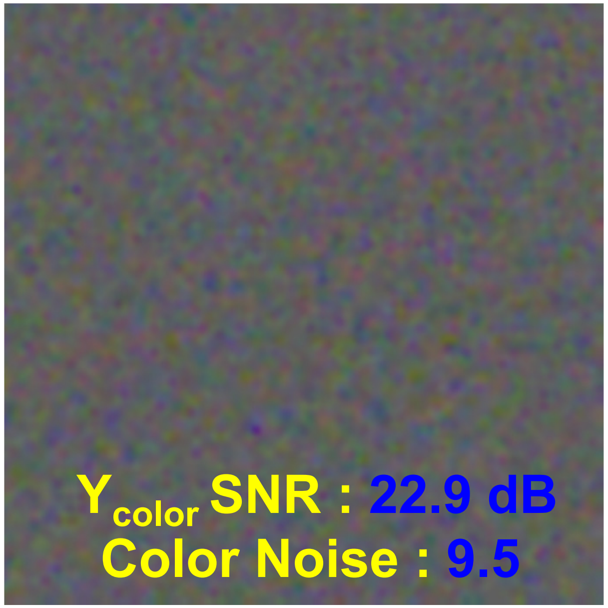
1.4um BSI | **1.12um BSI** | **1.12um F-DTI + VTG**





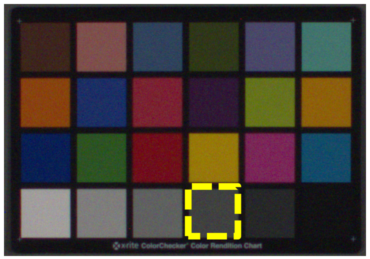


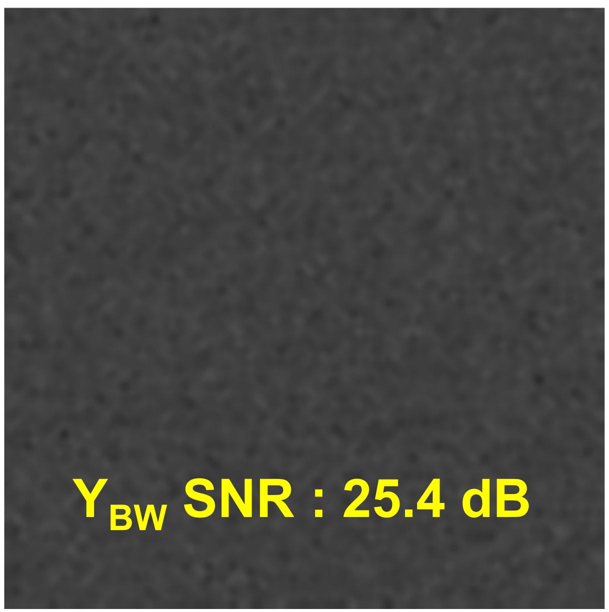




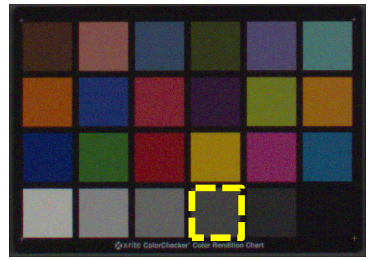
Low Crosstalk → High SNR

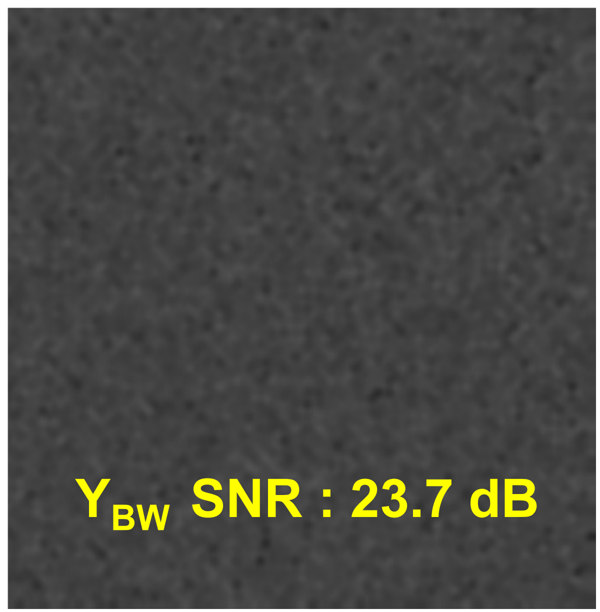
1.4um BSI



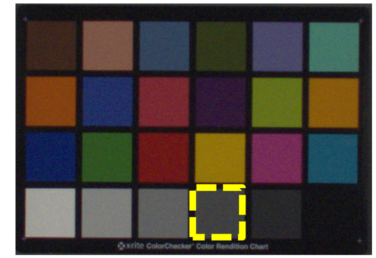


1.12um BSI





1.12um F-DTI + VTG



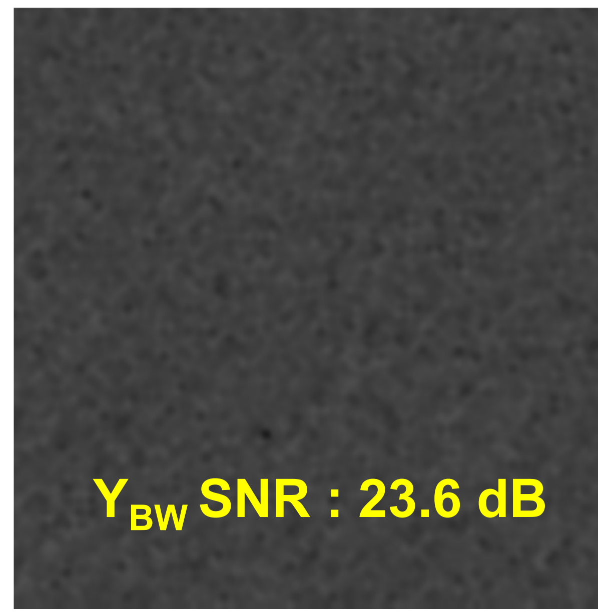


Image Comparison

Image Comparison

Chip Micrograph

Summary

- Small 3D BSI pixel having fully surrounding, full depth ***Front DTI and VTG*** is developed
  - SNR 30% improvement
  - Full well capacity 24% improvement
  - Zero silicon crosstalk and No blooming
  - Sensitivity improvement by lower F#
  - Smaller module height by increasing max CRA
- ***Front DTI with VTG in small size pixel*** will be the next key technology ***after BSI***

243.3pJ/pixel Bio-Inspired Time-Stamp-Based 2D Optic Flow Sensor for Artificial Compound Eyes

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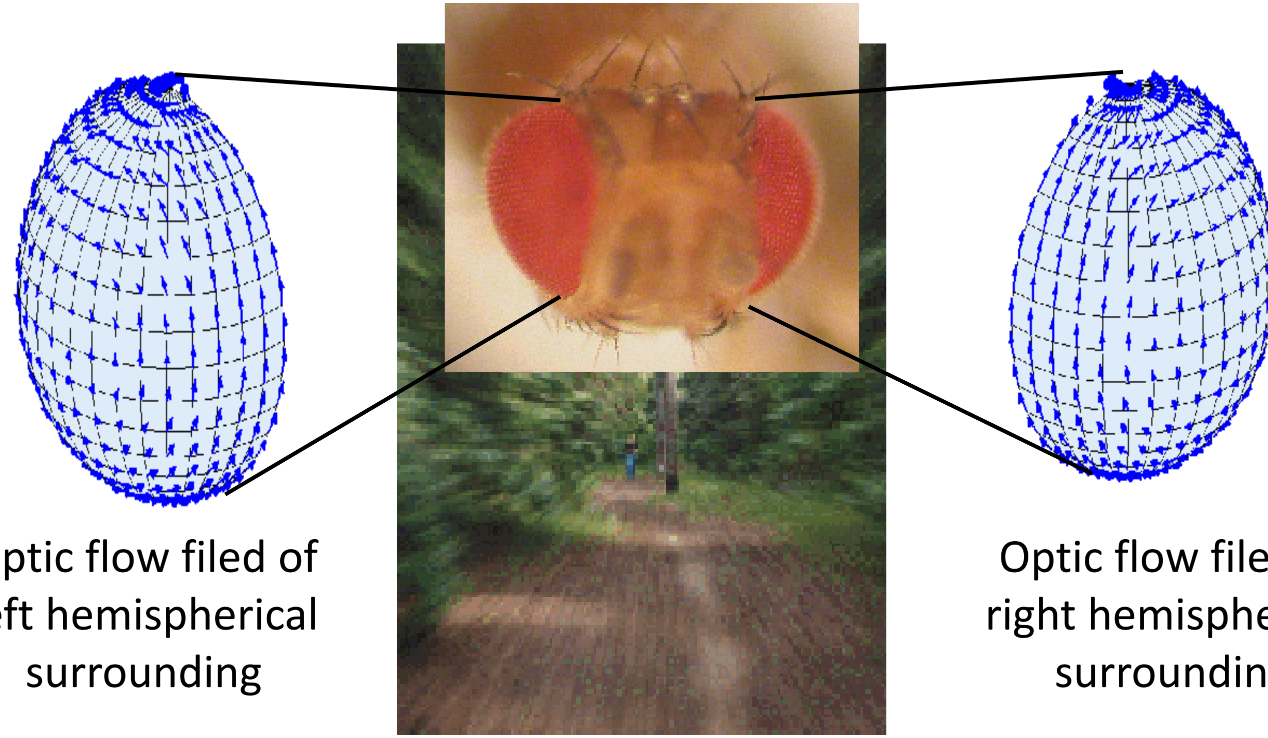
Department of Electrical Engineering and Computer Science
The University of Michigan, Ann Arbor, MI 48109

Outline

- Introduction
- System architecture
- Sensor design approach
  - ➢ Time-stamp-based optic flow sensing
  - ➢ Optic flow data compression
- Experimental results
- Summary

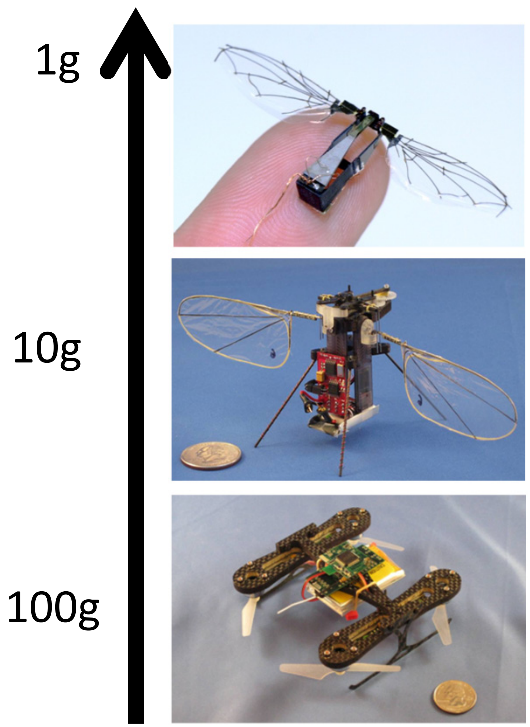
Compound Eyes



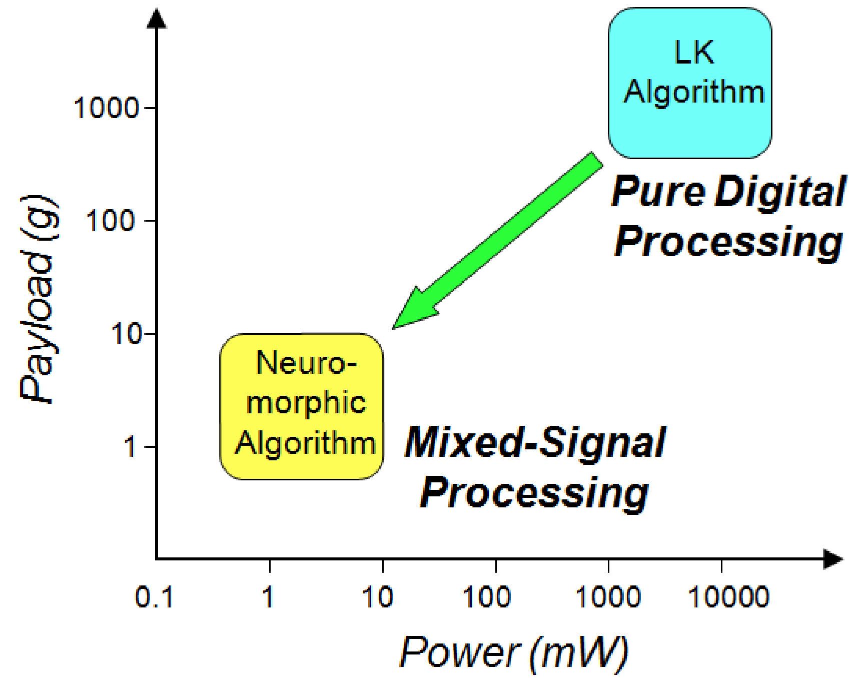
Compound eyes in a flying insect

- Wide field-of-view (FoV) optic flow sensing
- Speed, depth, and self-motion (ego-motion)
- Agile and safe navigation

Micro Air Vehicles (MAVs)



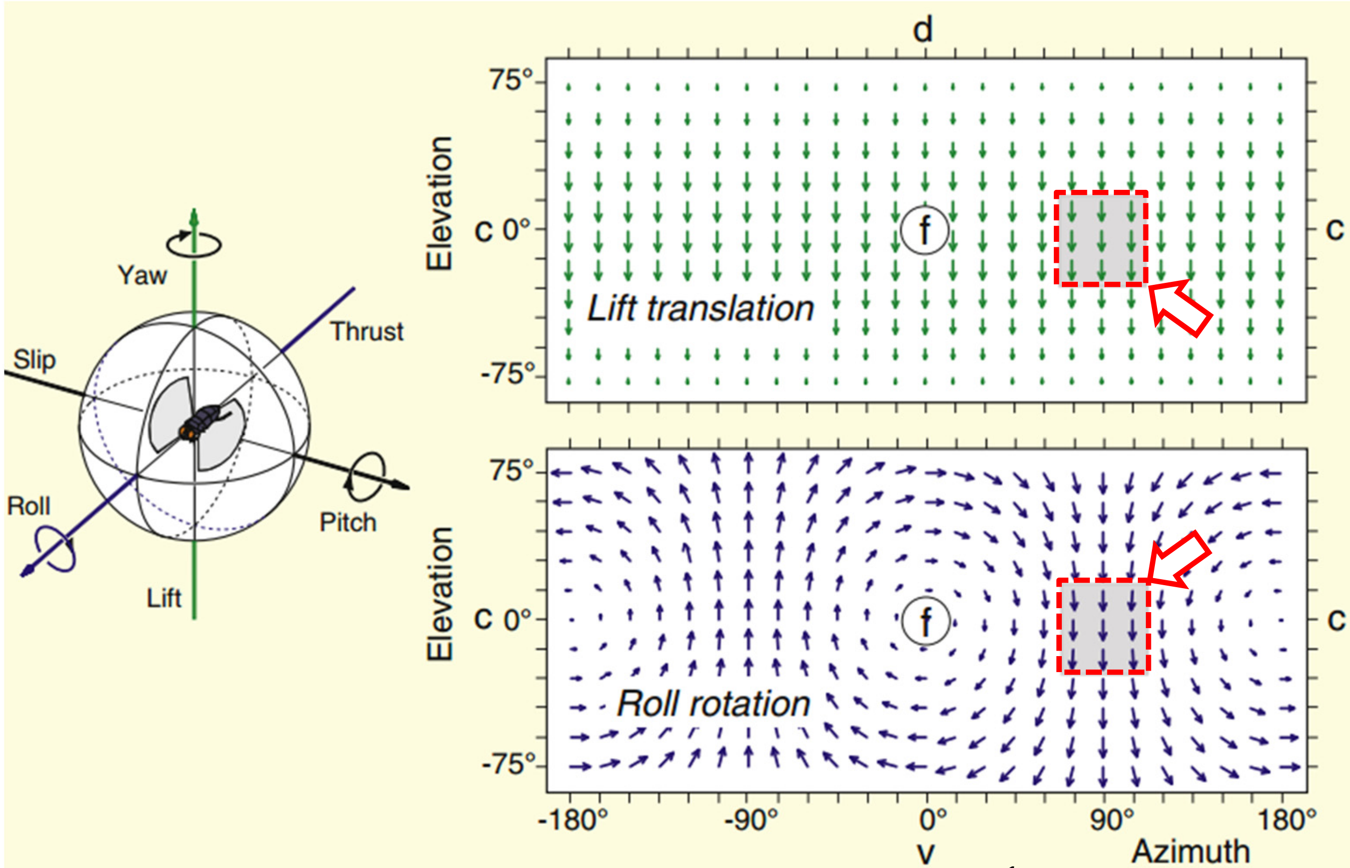
Micro air vehicles



Power vs. payload chart of optic flow sensor

- Smallest unmanned aerial vehicles
- Low payload and low power constraints
- GPS, ultrasonics (X) → wide FoV optic flow (O)

Self-Motion in Wide FoV Optic Flow



Same pattern from different motions

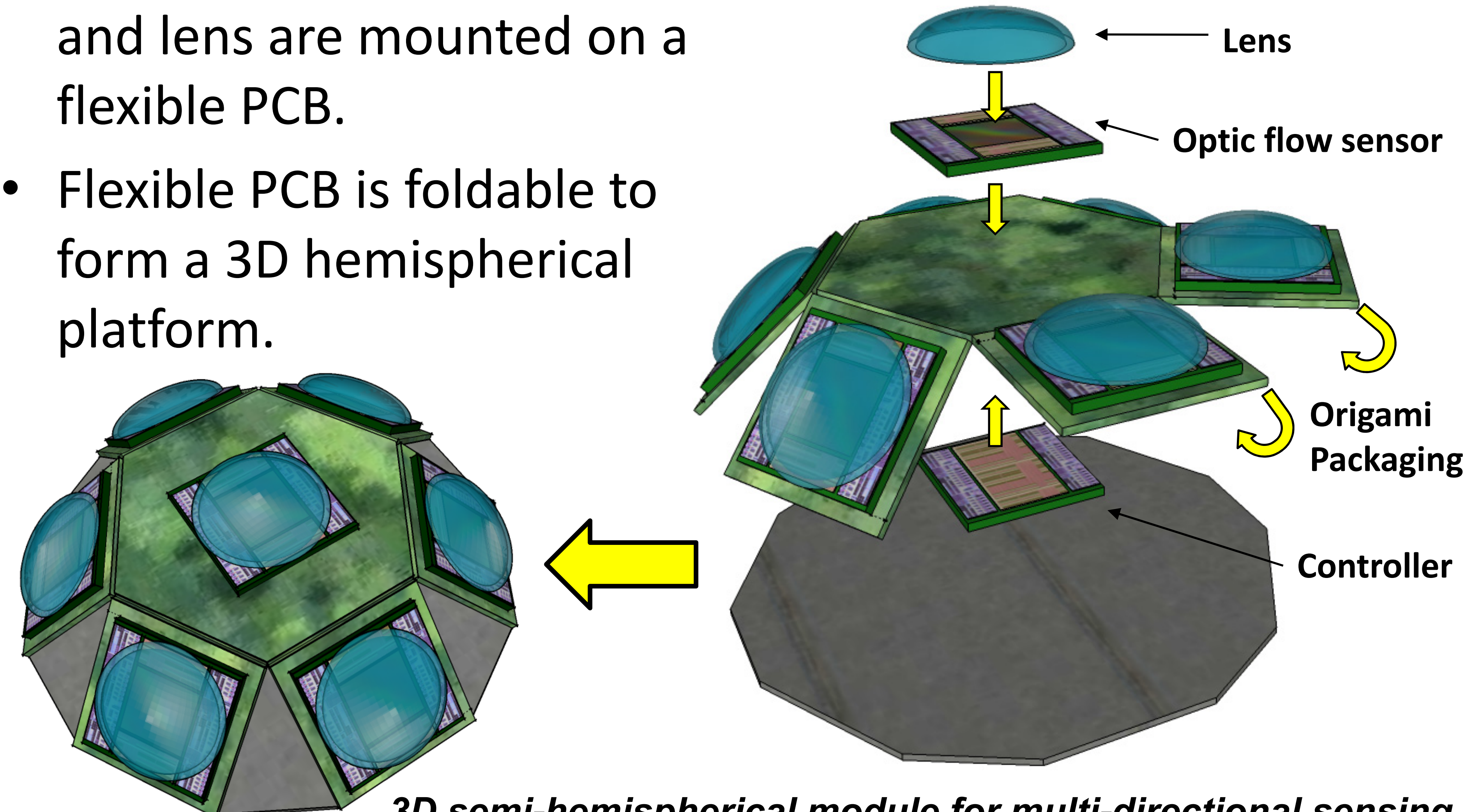
Fig. Self-motion and optic flow field[1]

- Wide FoV optic flow encodes self-motion.
- Local optic flow cannot distinguish self-motion.

[1]H. G. Krapp, "Sensory integration: neuronal adaptations for robust visual self-motion estimation.," *Current biology : CB*, vol. 19, no. 10, pp. R413–6, May 2009.

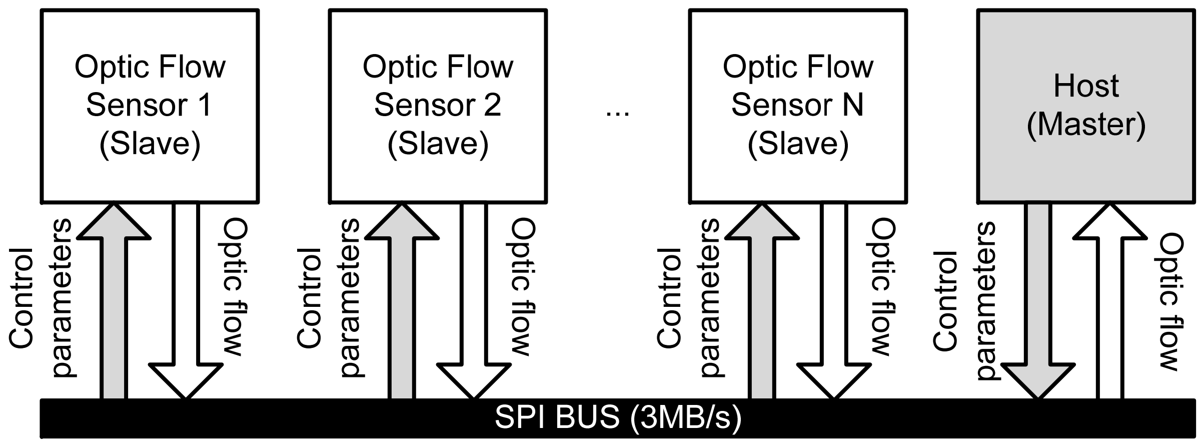
Artificial Compound Eye Platform

- Optic flow sensors, circuitry, and lens are mounted on a flexible PCB.
- Flexible PCB is foldable to form a 3D hemispherical platform.



3D semi-hemispherical module for multi-directional sensing

System Architecture



Control parameters

- Algorithm parameters
- Signal bypass

Optic flow

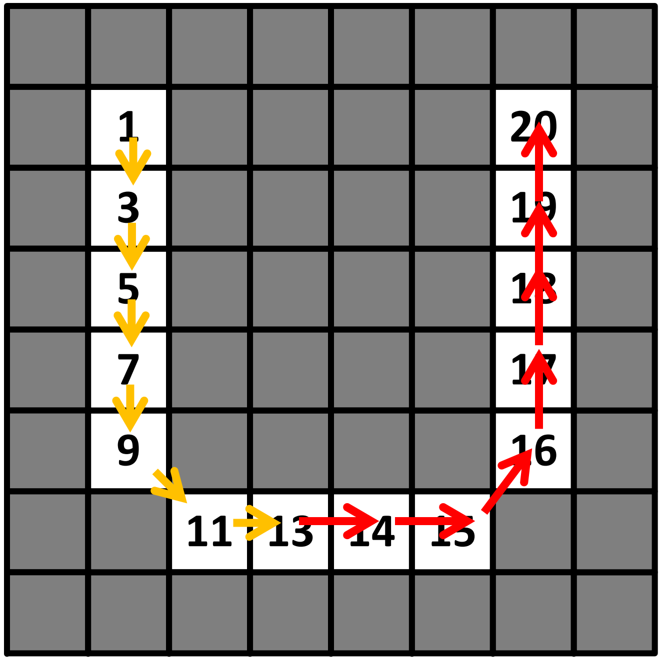
- 1-b serialized raw or compressed optic flow

Two design constraints for optic flow sensors

- Low power 2D optic flow core
  - **Bio-inspired 2D time-stamp-based optic flow estimation algorithm**
  - Reduce calculation power
- Low output data bandwidth for multiple sensors
  - 4-wired SPI bus (3MB/s)
  - **Lossless data compression** enables 25 sensors can send full resolution data.

Time-Stamp Information

0.5 pixel/frame

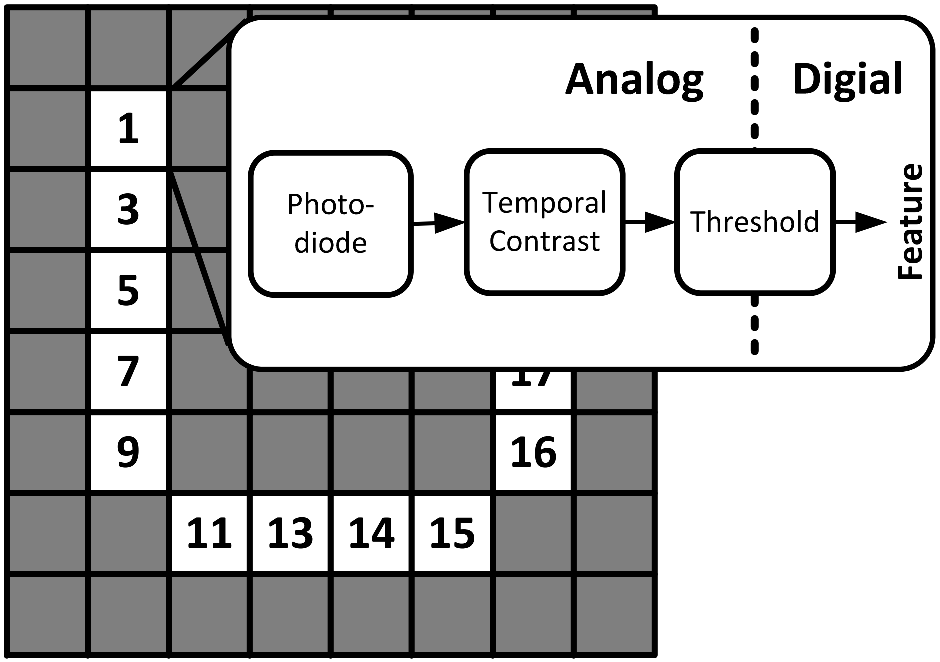


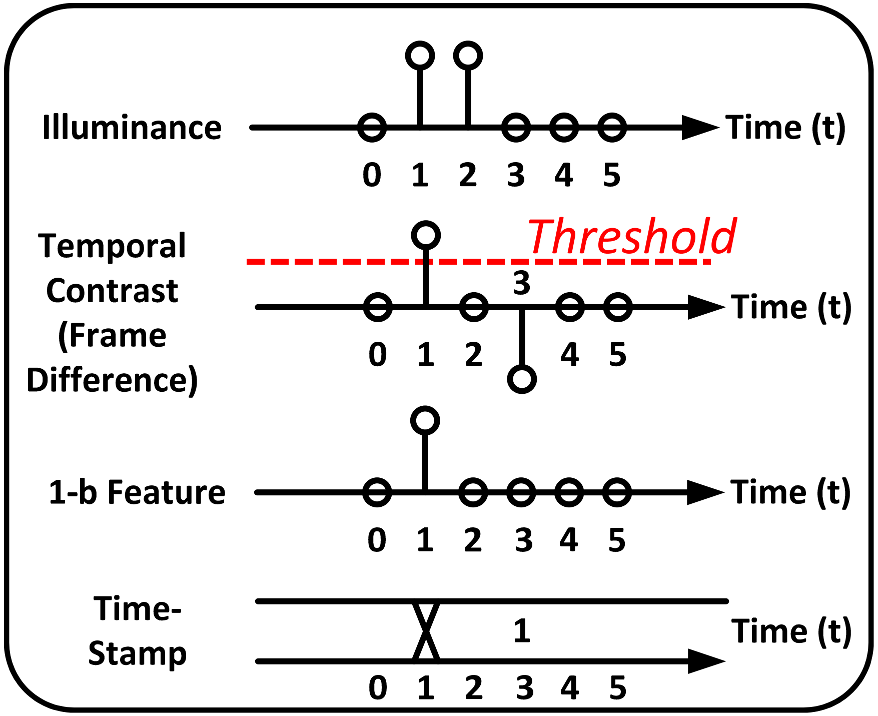
1 pixel/frame

Faster

- Time-stamp information is the time when a moving object came into the pixel.

Moving Feature Arrival Detection

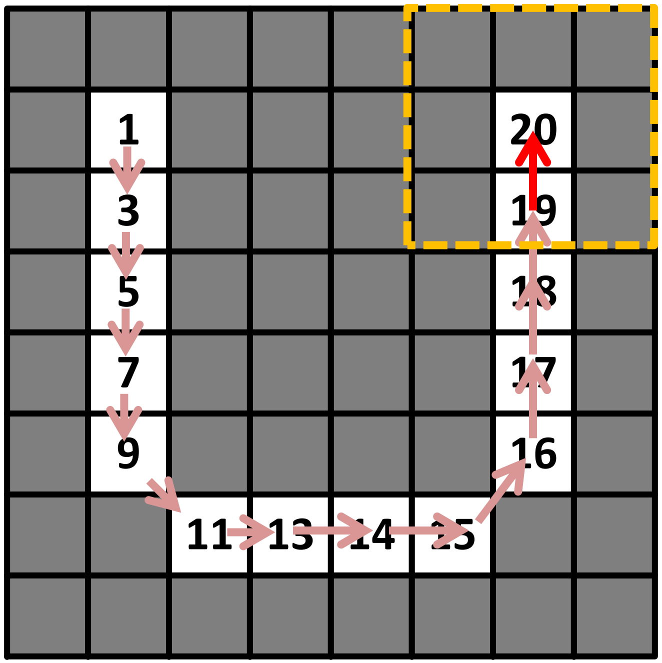




- Temporal contrast change & thresholding at each pixel detects the entrance of a moving feature.
- 1-b feature updates time-stamp value.

Velocity Measurement

@t=20 (frame counter)



$T_x = 0$

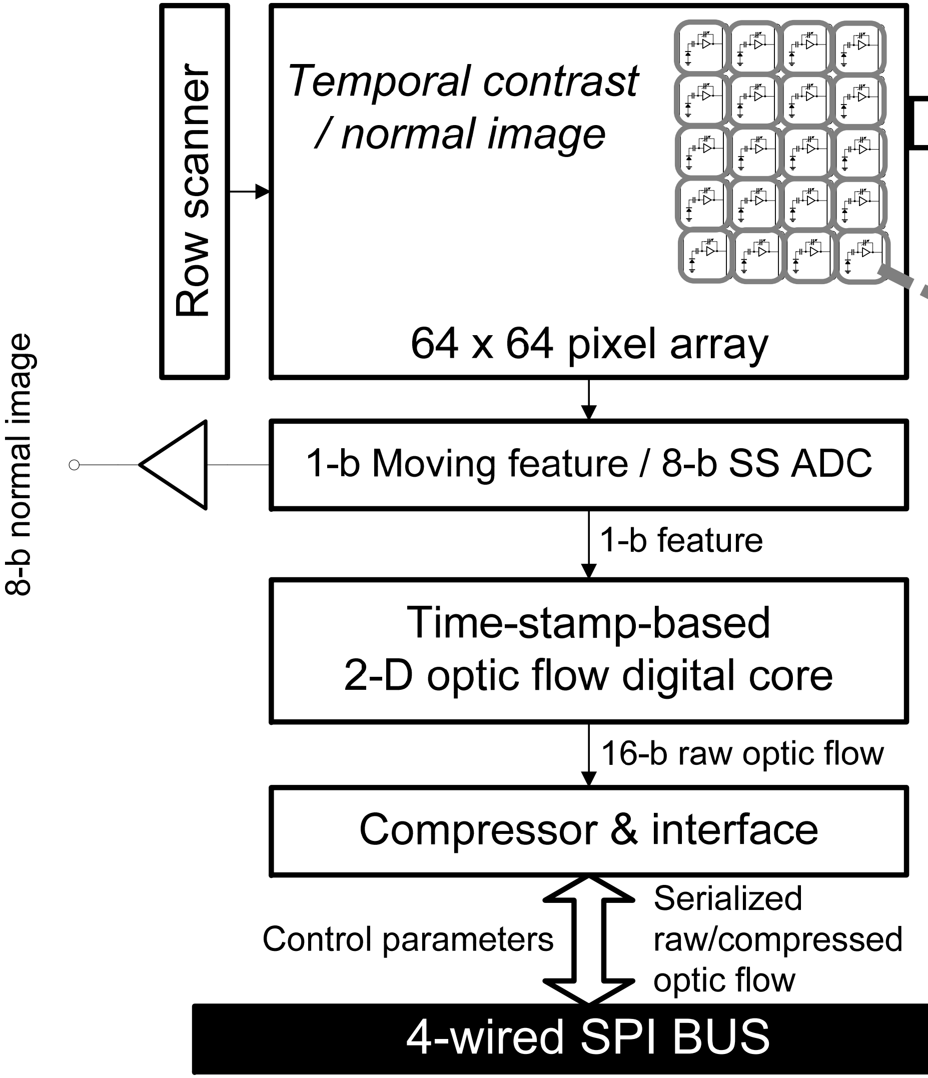
$T_y = 19-20 = -1$[frame/pixel]

$V_x = 0$

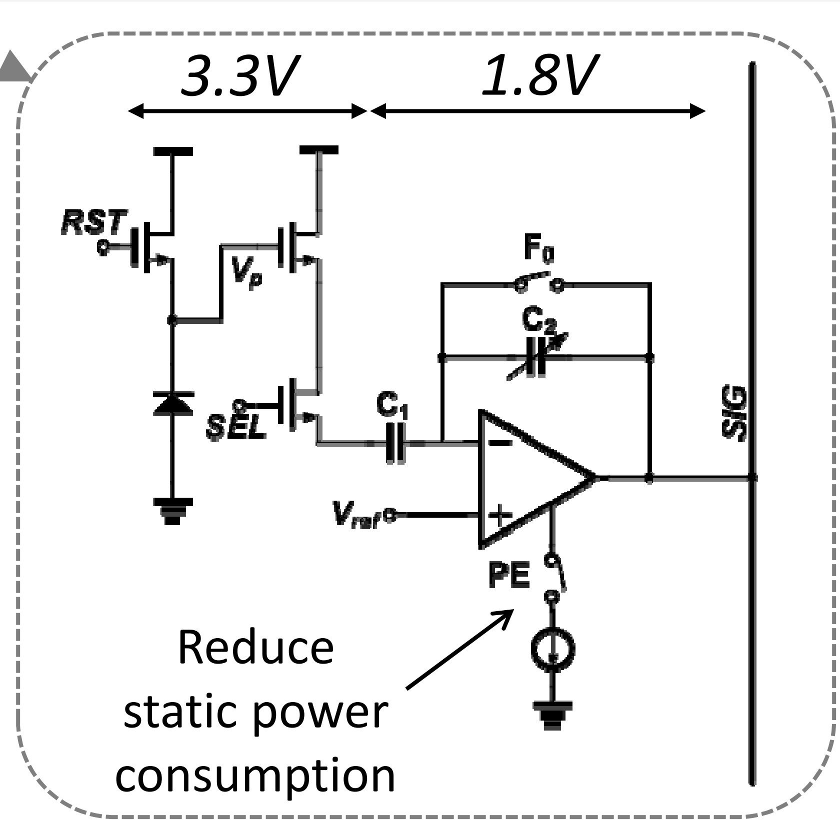
$V_y = -1$[pixel/frame]

- Time-of-travel (T_x, T_y) measured by subtraction of time-stamp information.
- Velocity (V_x, V_y) = 1/time-of-travel [pixel/frame]

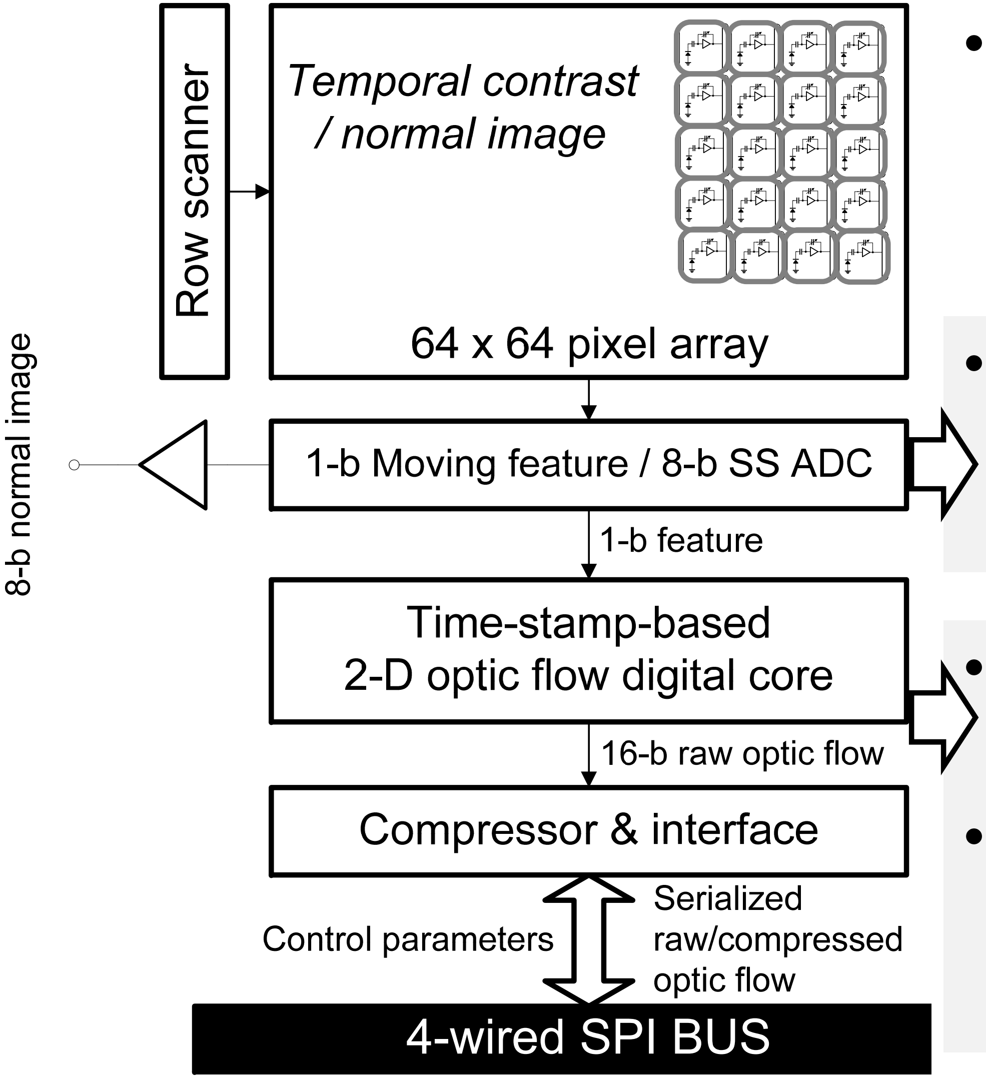
Sensor Architecture: Pixel



- In-pixel discrete-time HPF (1.8V supply)
  - Measure contrast change

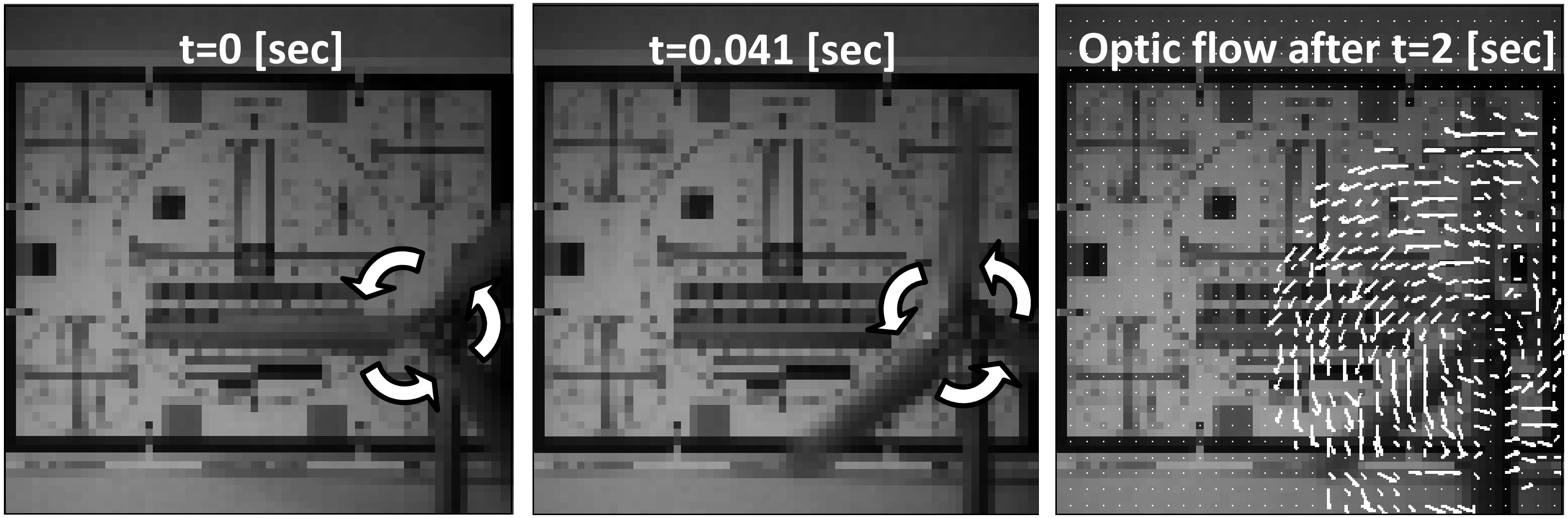


Sensor Architecture: Digital Processing

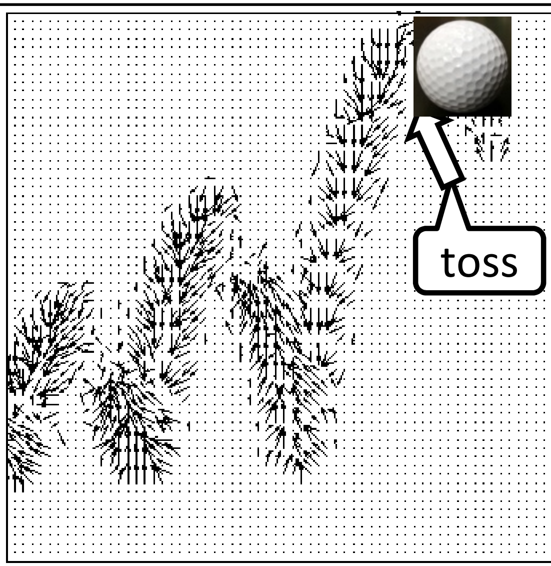


- In-pixel discrete-time HPF (1.8V supply)
  - Measure contrast change
- Column-level 1-b comparator (0.9V supply)
  - Feature detection
- Time-stamp-based 2D optic flow estimation core
- Peripheral circuits
  - Lossless data compressor
  - SPI

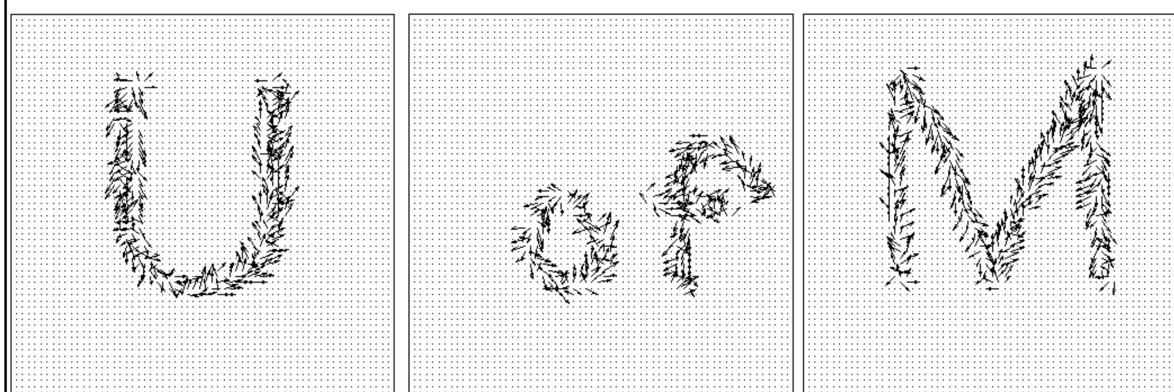
Sample Images



2-D optic flow from a rotating fan (120fps)

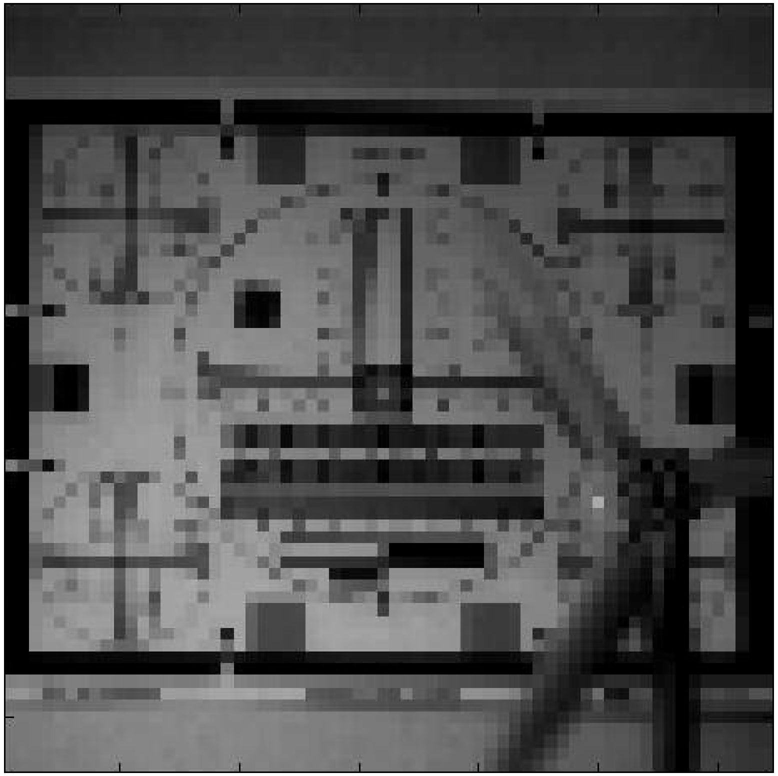


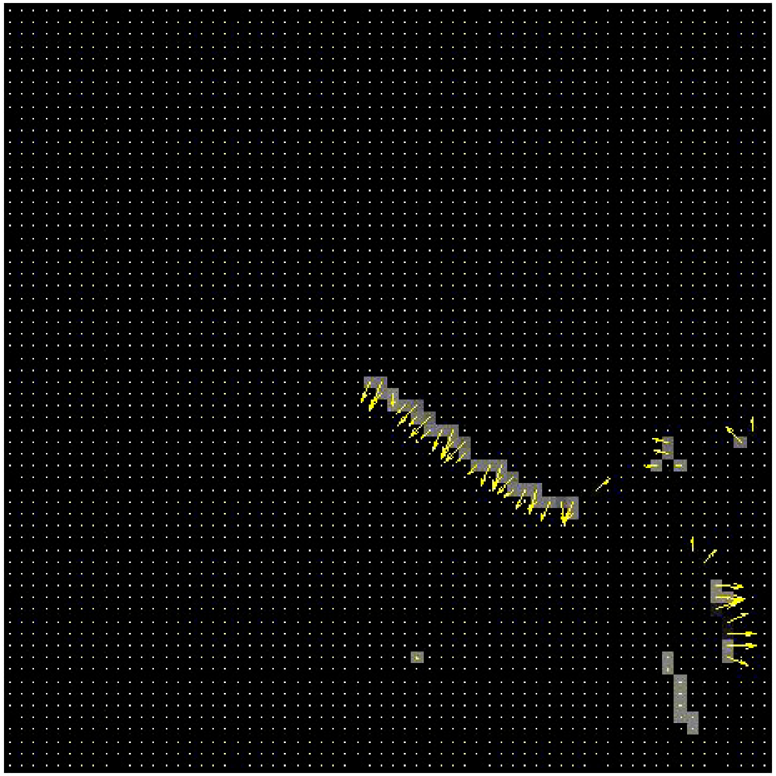
Bouncing ball: captured @120fps



Letters by tracing a laser pointer source: captured @60fps

Sample Video: Rotating Fan

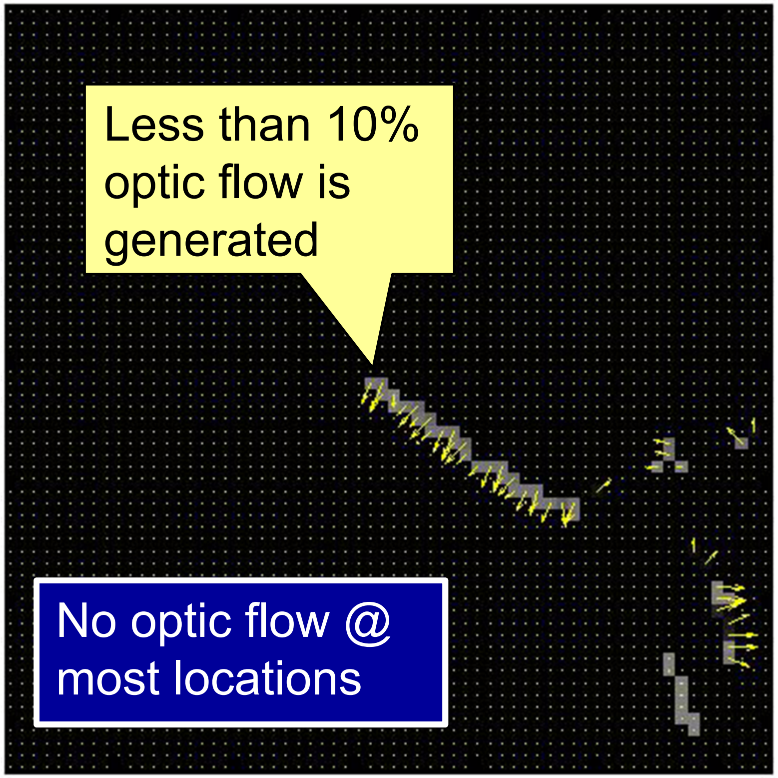




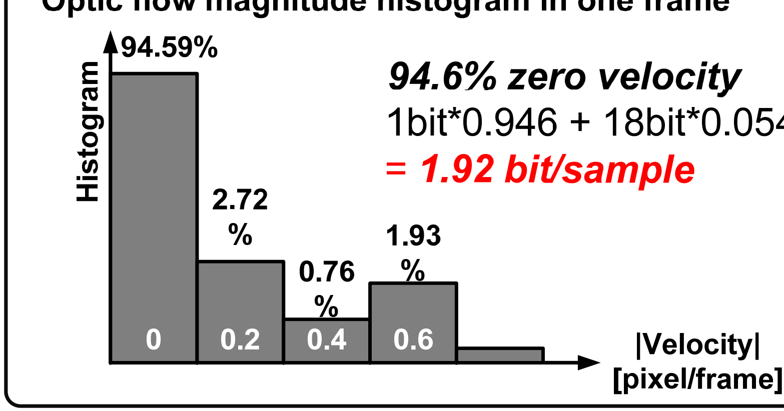
2-D optic flow from a rotating fan
(captured @120fps, displaying @15fps)

Lossless Optic Flow Data Compression

Data from a virtual fly robot simulator



Measured optic flow from a rotating fan

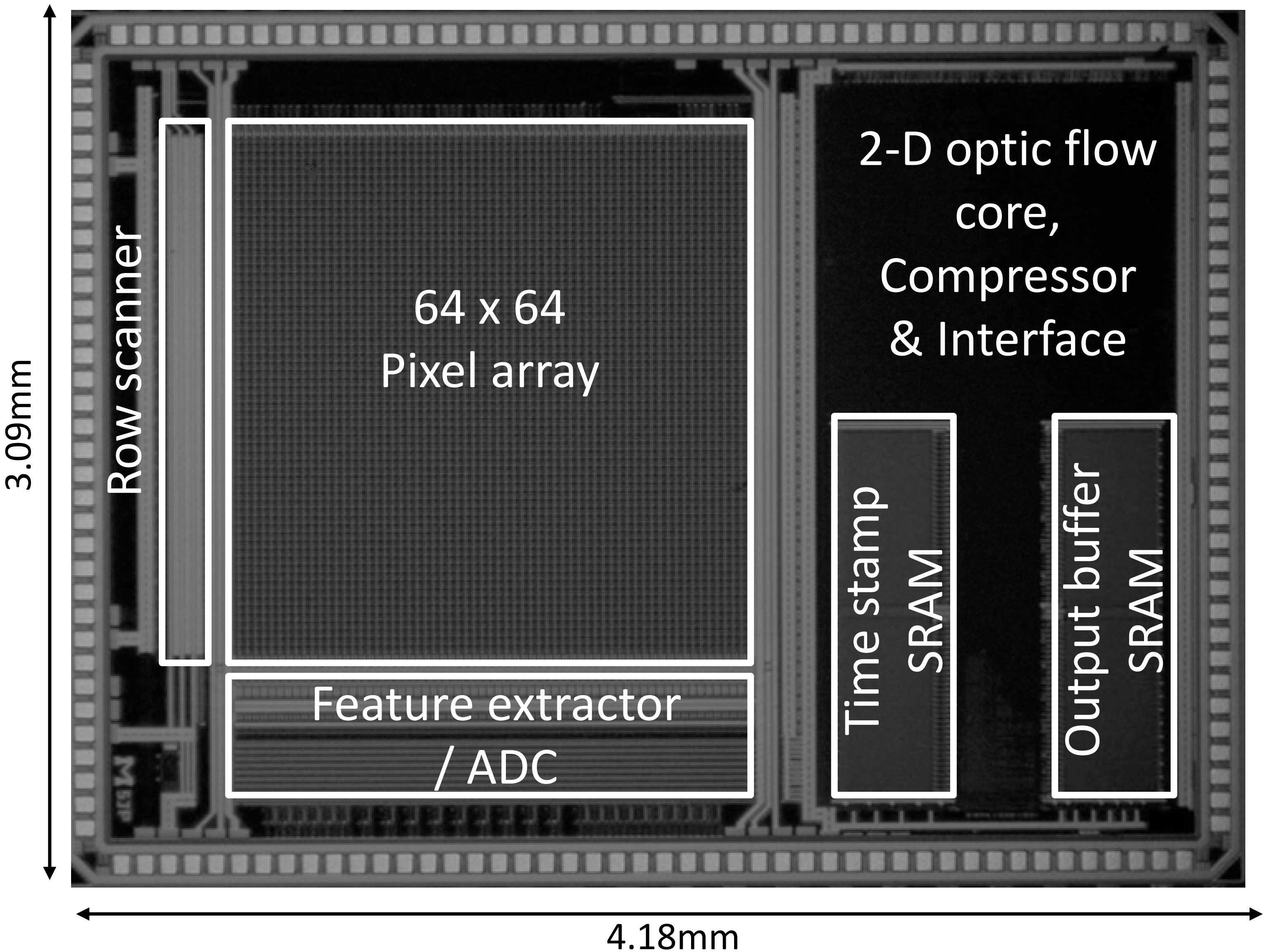


Compression algorithm: Pseudo code

```
If '0' velocity
{
    Send 1-b '1' code;
}
else
{
    Send 2-b header ('01') + 16-b raw optic flow;
}
```

- **More than 8 times data reduction**
  - 3 sensors per module → 25 sensors @ 3MB/s SPI

Chip Micrograph



Chip Characteristics

Process	0.18 µm 1P4M CMOS		
Chip size	4.18 x 3.09 mm^2		
Pixel array	64 x 64		
Pixel size	28.8 x 28.8 μm^2		
Fill factor	18.32 %		
Maximum optic flow	1.96 rad/sec @ 120 fps, FOV 60º		
Power (Pixel, 3.3V @ 30 fps)	0.57 µW	2-D optic flow estimation	29.9 µW
Power (ADC 1.8 V analog, 0.9V digital @ 30 fps)	5.30 µW		
Power (2-D optic flow core, 1.8 V, @ 30 fps)	**24.03 µW**		
Power (Compressor & interface, 1.8 V, @ 30 fps)	**79.48 µW**		
Total power (@ 30fps)	109.38 µW		
Optic flow data rate after compression (16-b/sample raw data)	Average: 1.92-b/sample Peak: 4.84-b/sample (< 2.77% occurrence frequency)		

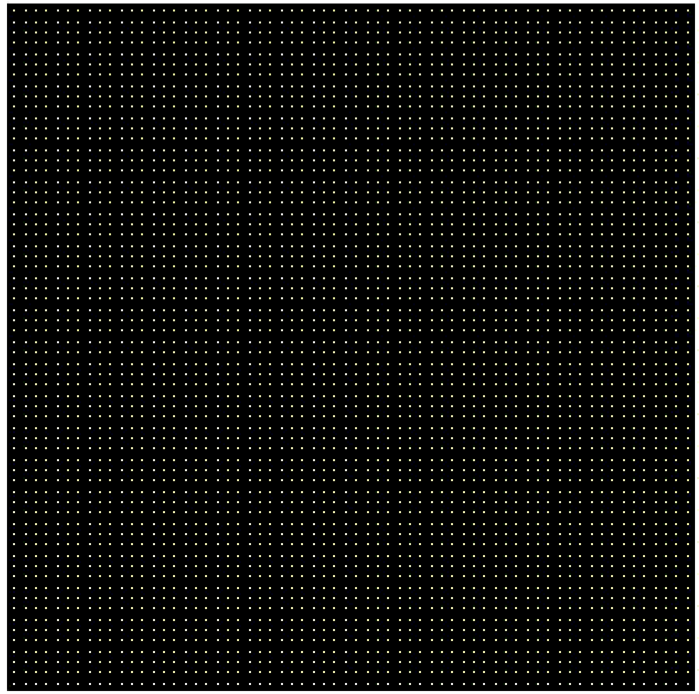
Summary

- Artificial compound eyes: multi-directional optic flow sensing
  - 243.3pJ/pixel 2D optic flow sensing core
  - 4-wired SPI bus
- Bio-inspired low power 2D optic flow computation
  - Moving feature detection
  - Time-stamp-based optic flow estimation
- Lossless optic flow data compression
  - Up to 25 sensors per 3MB/s SPI with full resolution data transmission (64x64, 120fps)

Acknowledgements

- This research was supported by the U.S. Army Research Laboratory under contract W911NF and prepared through collaborative participation in the microelectronics Center of Micro Autonomous Systems and Technology (MAST) Collaborative Technology Alliance (CTA).
- Rackham Graduate School of University of Michigan supported travel grants for the trip.

Sample Videos: U of M



Letters by tracing a laser pointer source: captured @60fps

Thank you for your attention.

A 1000fps Vision Chip Based on a Dynamically Reconfigurable Hybrid Architecture Comprising a PE Array and Self-Organizing Map Neural Network

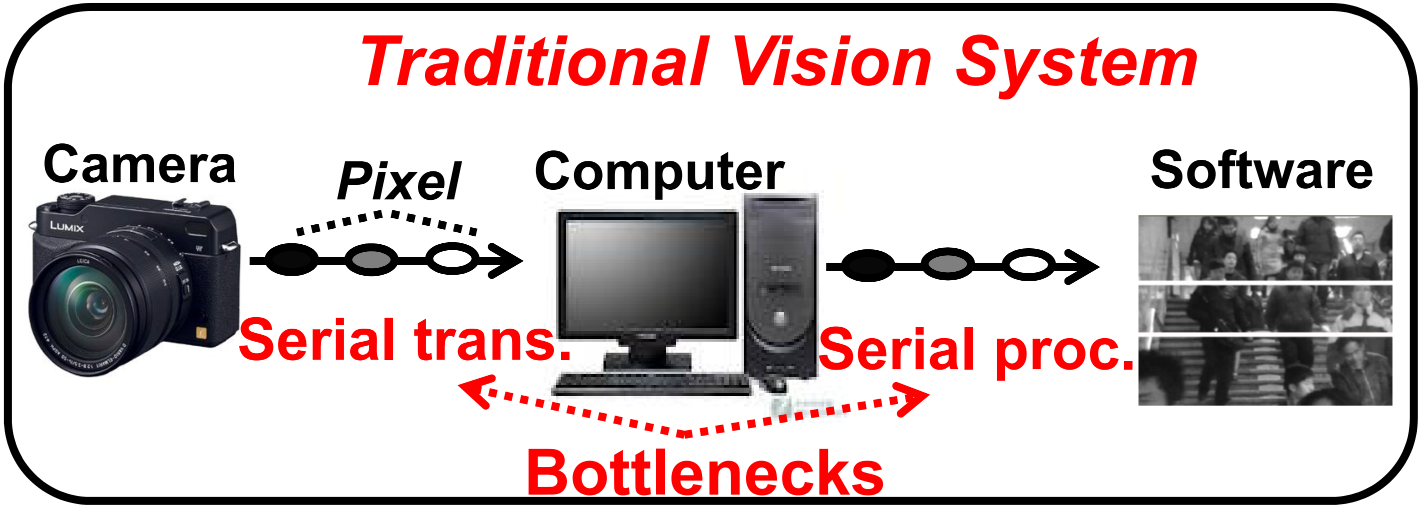
Cong Shi[1,2], Jie Yang[1], Ye Han[1], Zhongxiang Cao[1], Qi Qin[1], Liyuan Liu[1], Nan-Jian Wu[1*], Zhihua Wang[2]

[1]*Chinese Academy of Sciences, Beijing, China*
[2]*Tsinghua University, Beijing, China*

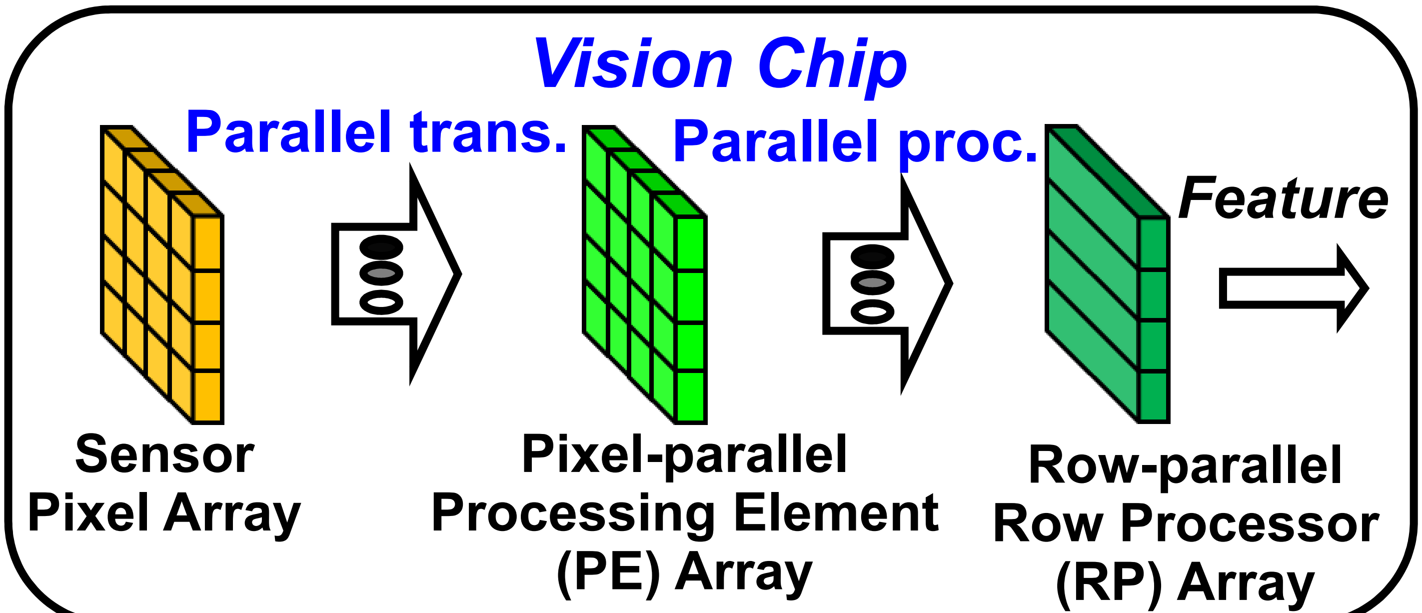
Outline

- Background
- Chip Architecture
  - System Architecture
  - Hybrid Processors with Multi-level Parallelism
  - Dynamic Reconfiguration for Neural Network
  - Flexible Pixel-Processor Mapping
- Design of Main Circuits
- Measurement Results
- Summary

Background

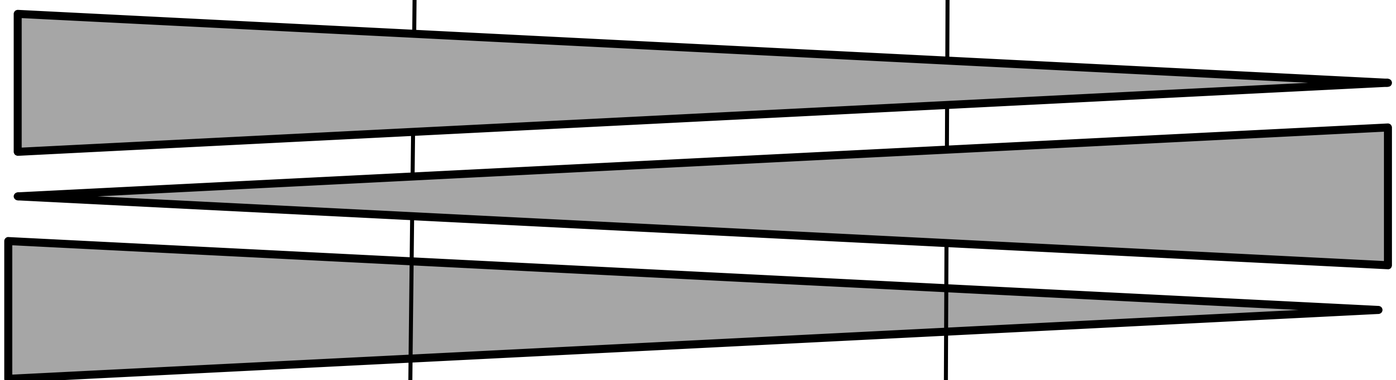
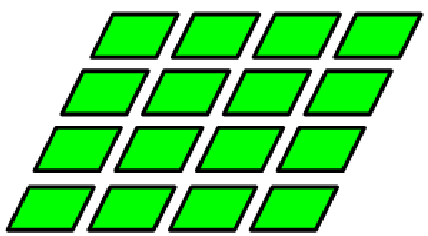
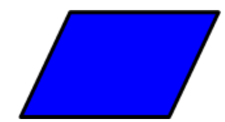


Not real-time
(<30fps)



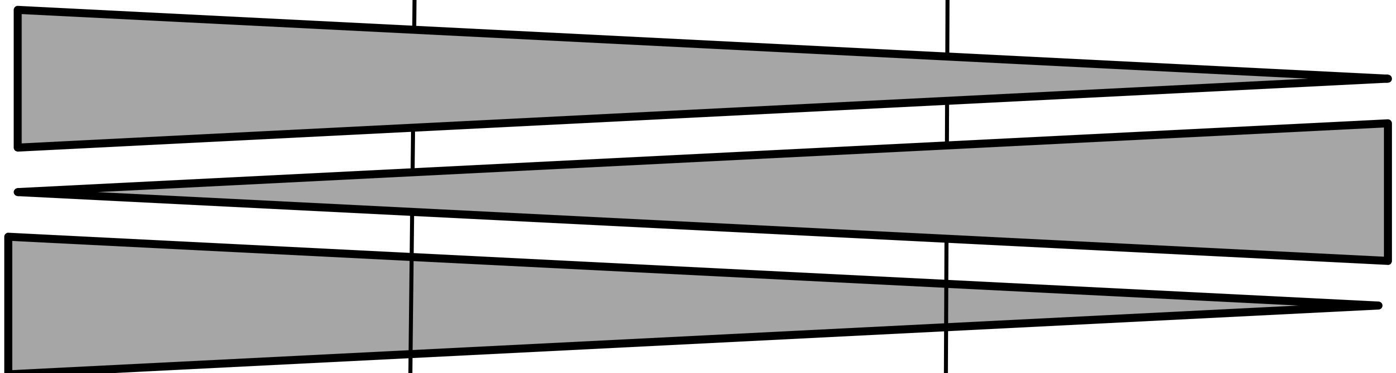
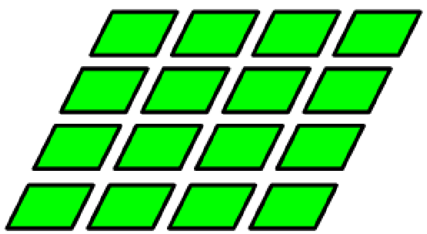
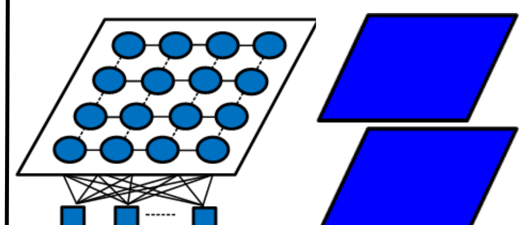
Real-time
(>1000fps)

Background: Big Challenge

Proc. Level	Low-level (Image filter.)	Mid-level (Feature extract.)	High-level (Feature recog.)
Parallelism *Complexity* *Data Size*			
Processors	 PE Array	 RP Array	 MPU
Speed	○	○	✖

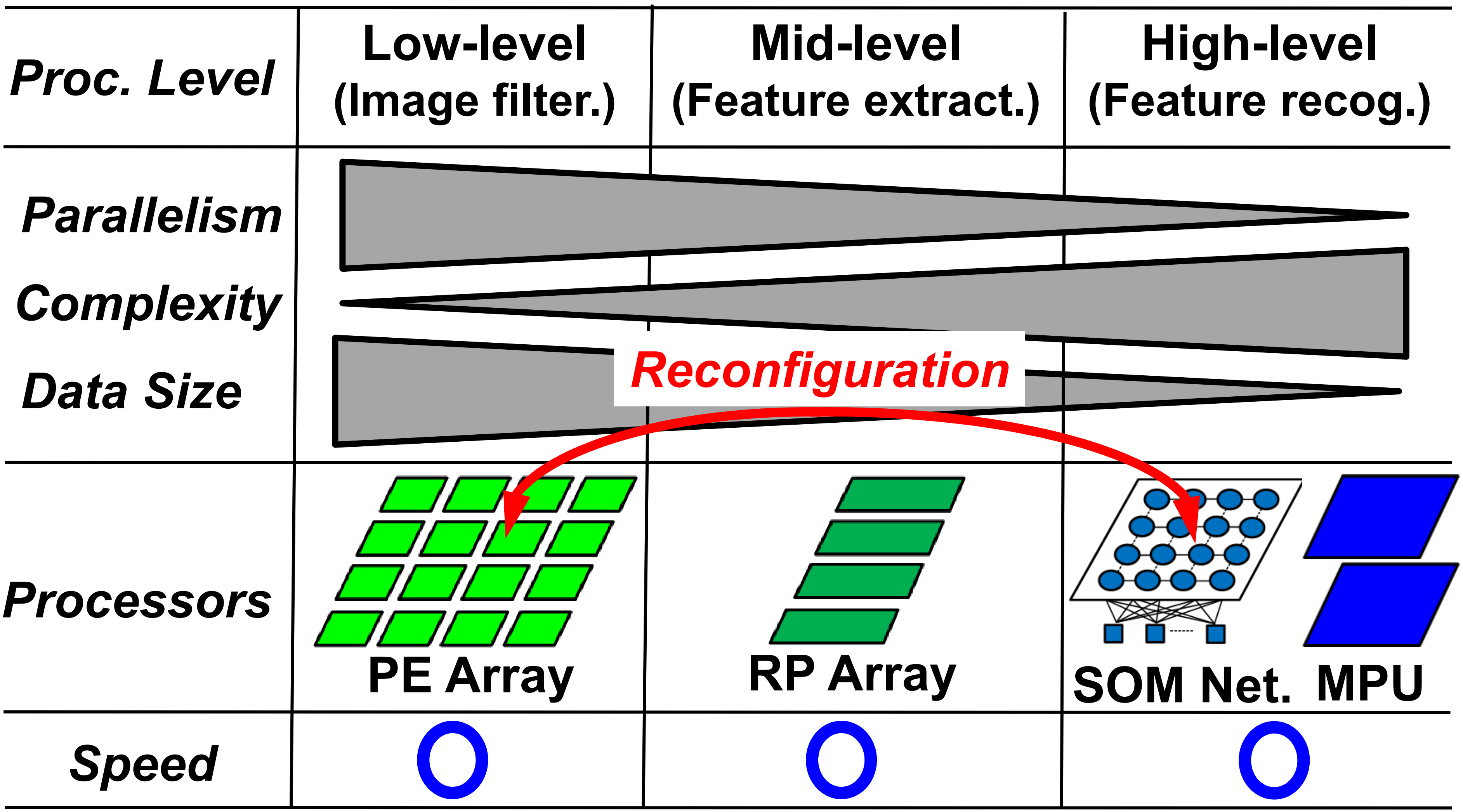
MPU: Mismatch with the proc. speed of PE &RP arrays,
System performance degradation to <<1000fps

Background: Our Approach

Proc. Level	Low-level (Image filter.)	Mid-level (Feature extract.)	High-level (Feature recog.)
Parallelism *Complexity* *Data Size*			
Processors	 PE Array	 RP Array	 SOM Net. MPU
Speed	○	○	○

- Parallel neural network for recognition speedup
- Dynamic reconfiguration for area budget reduction

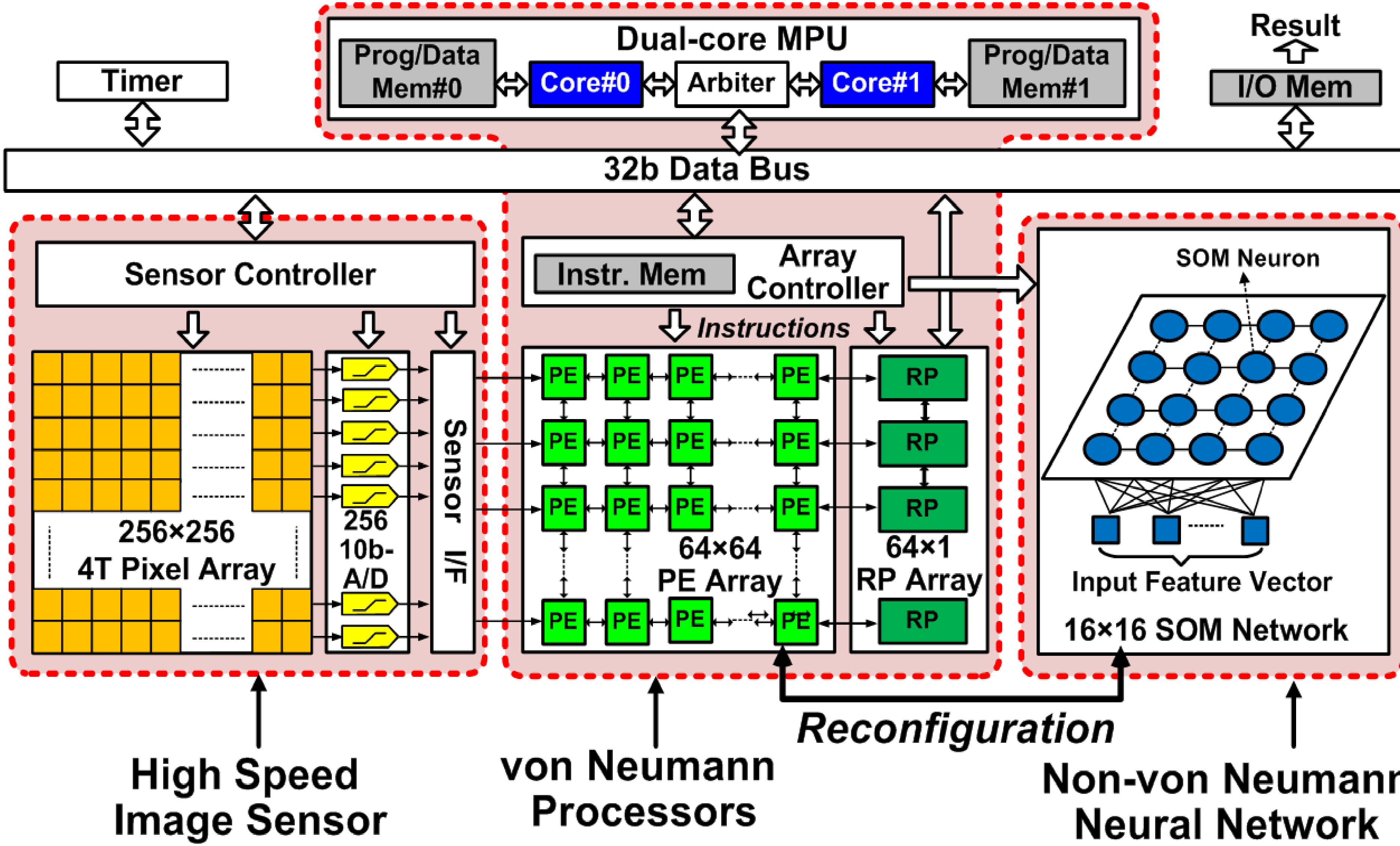
Background: Our Approach



- Parallel neural network for recognition speedup
- Dynamic reconfiguration for area budget reduction

Chip Architecture

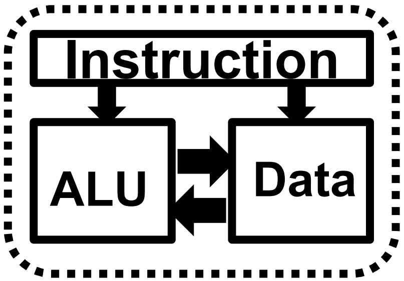
System Architecture



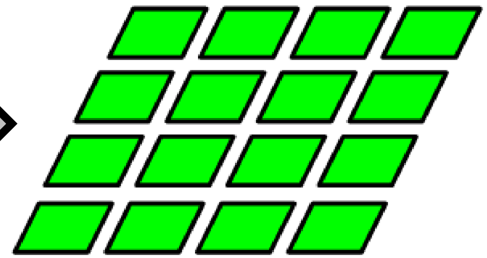
Chip Architecture

Hybrid Processors with multi-level parallelism

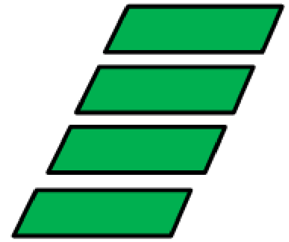
Von Neumann-Type Processors



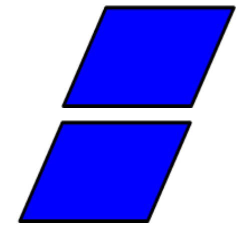
- Instruction driven
- precise operation



PE Array Processor (pixel-parallel)

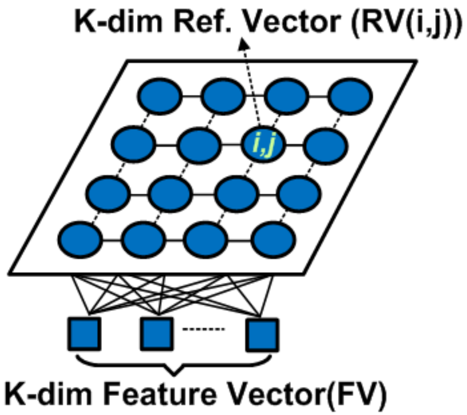


RP Array Processor (row-parallel)



Dual-core MPU (thread-parallel)

Non-von Neumann-Type Processor



SOM Neural Network (vector-parallel)

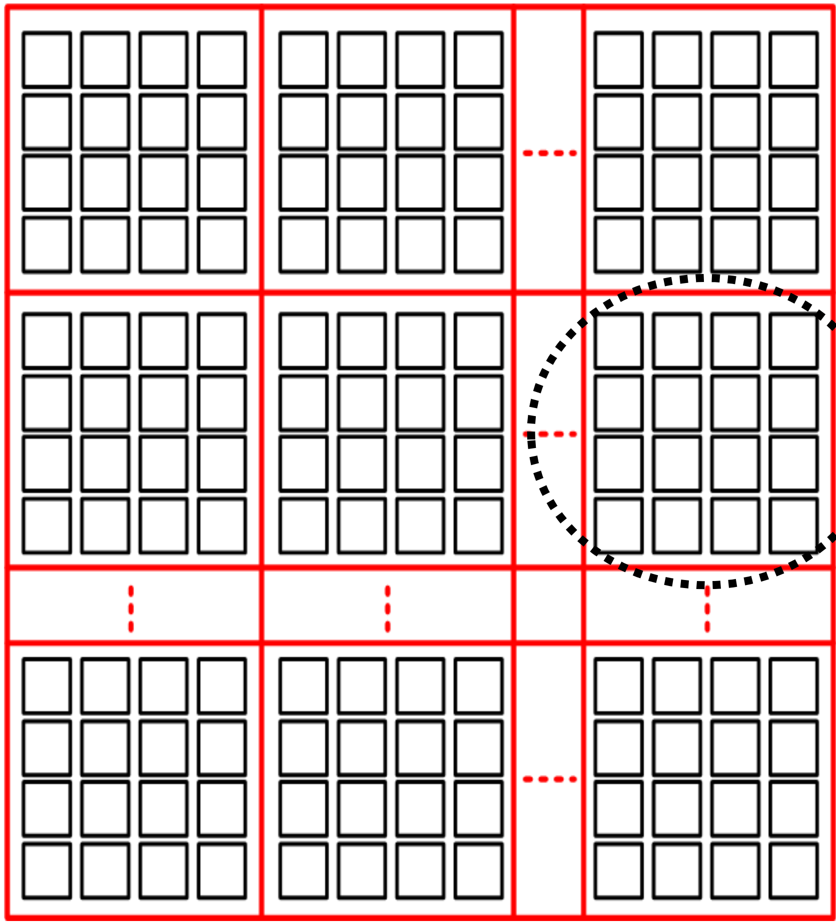
- *SOM Training*
  Online LVQ
- *SOM Recognition :*
  (i*, j*) = argmin ||RV(i, j)-FV||

- Data driven
- intuitive operation

Chip Architecture

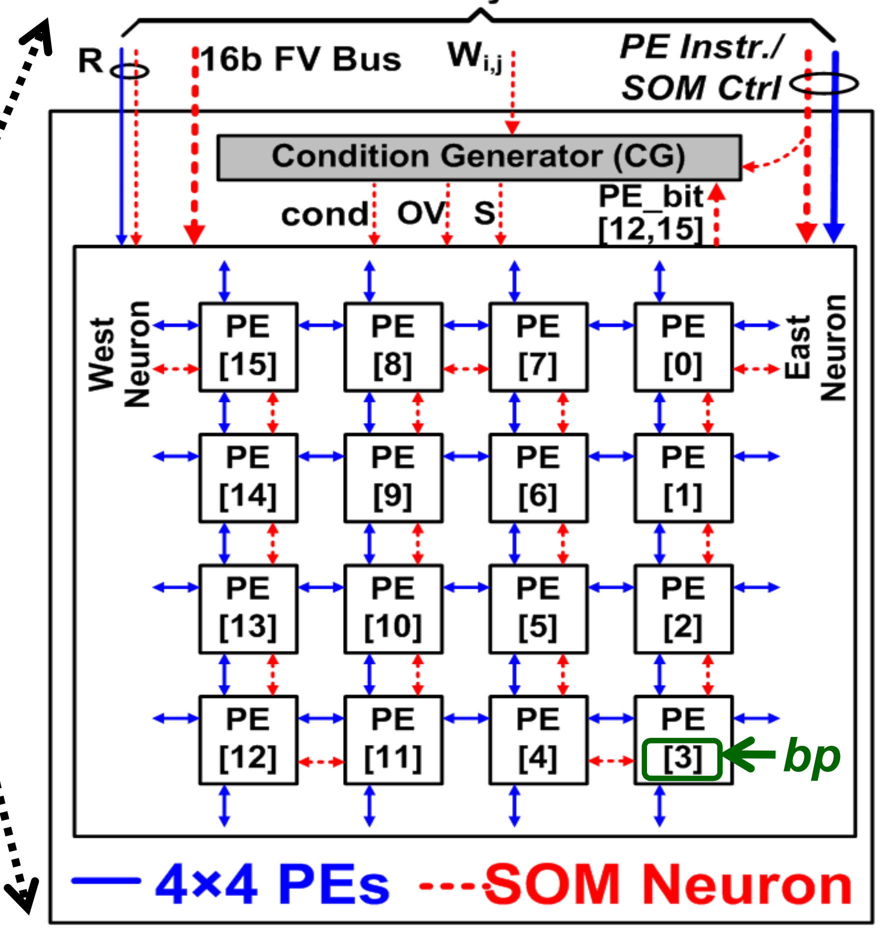
Dynamic Reconfiguration for Neural Network

64×64 PE Array



Partitioned into 16x16 subarrays

One Neuron

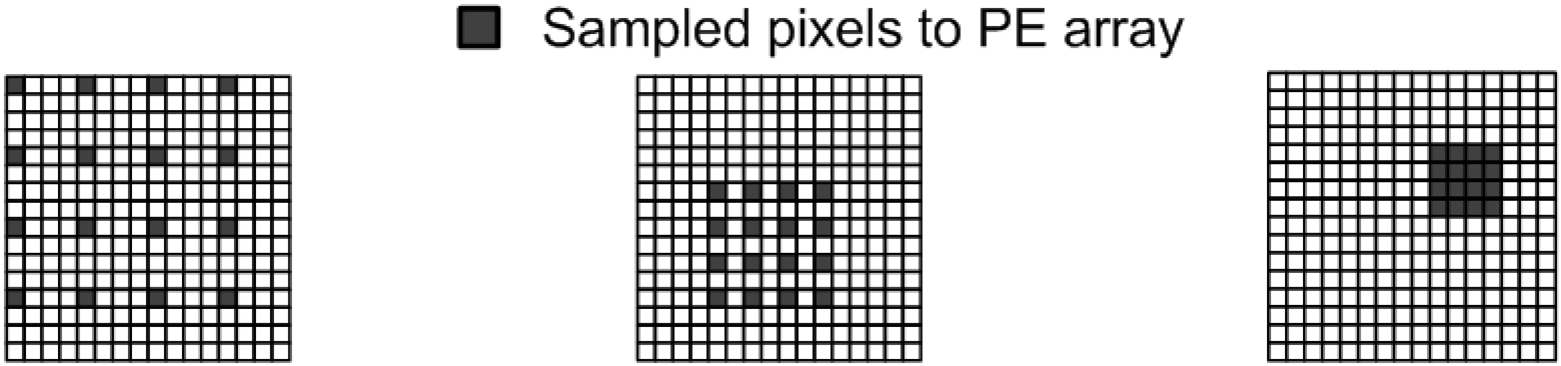


R signal switches path connections and controls the reconfiguration.

Chip Architecture

Flexible Pixel-Processor Mapping

Flexible Pixel-PE mapping relationship



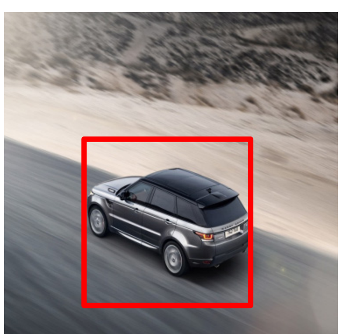
4:1 sample in whole **256×256** region

2:1 sample in arbitrary **128×128** region

1:1 sample in arbitrary **64×64** region

Bio-inspired *Glance* – *Stare* Scheme

Glance

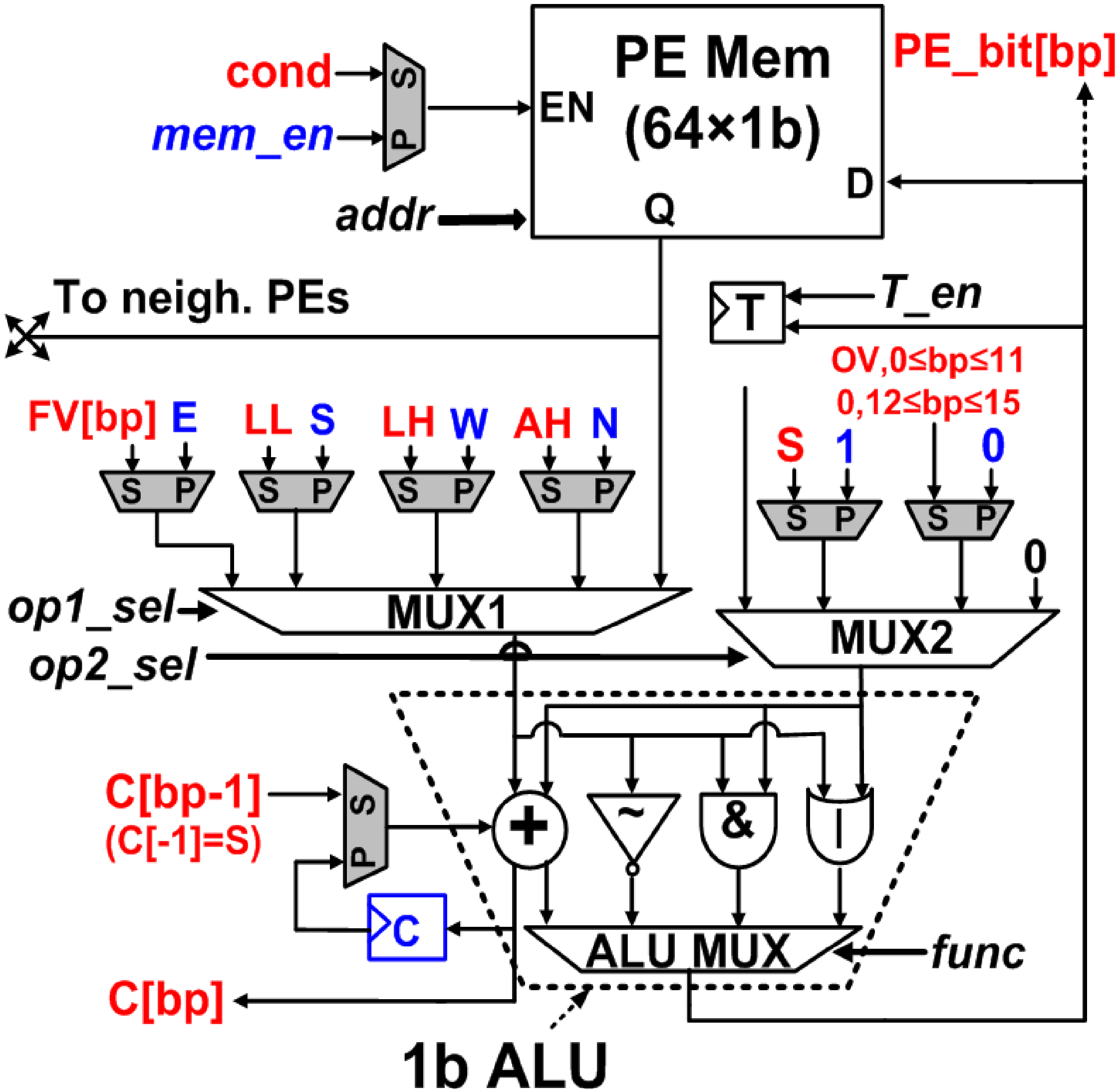


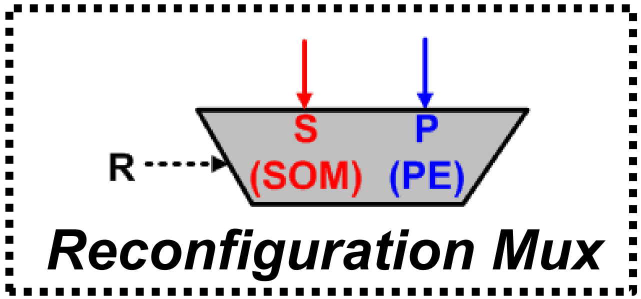
Locate object of interest

Stare

Focus on object

Design of Main Circuits: PE





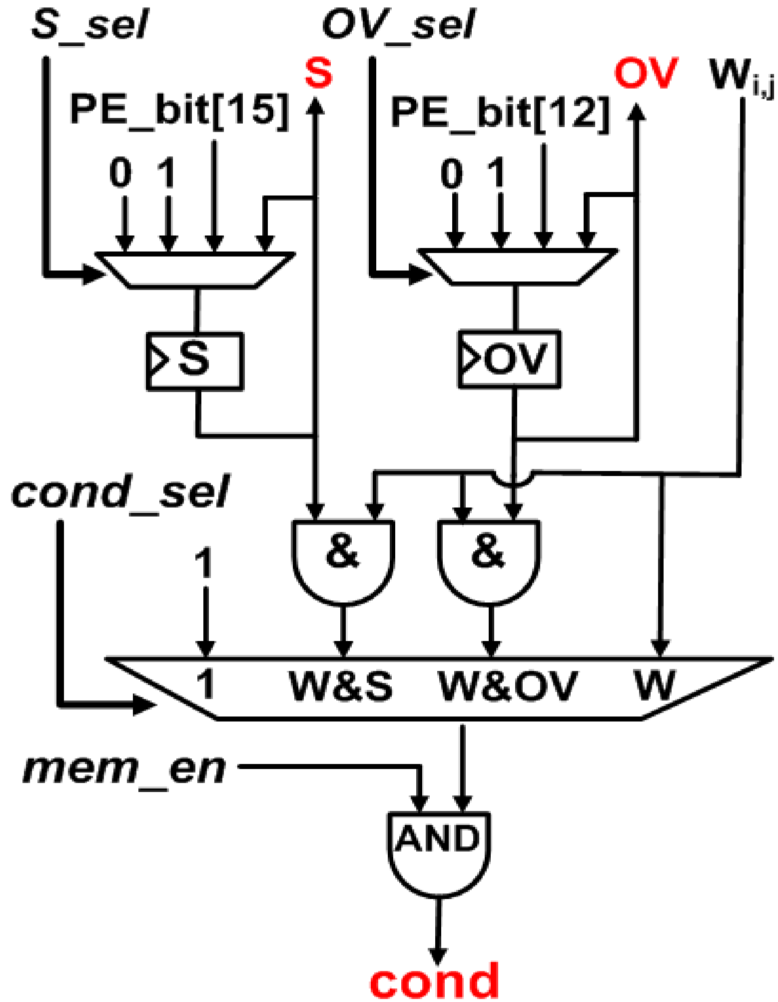
PE mode:

- 1b ALU operation
- Multi-bit operation in bit-serial

SOM mode:

- 16b operation in bit-parallel

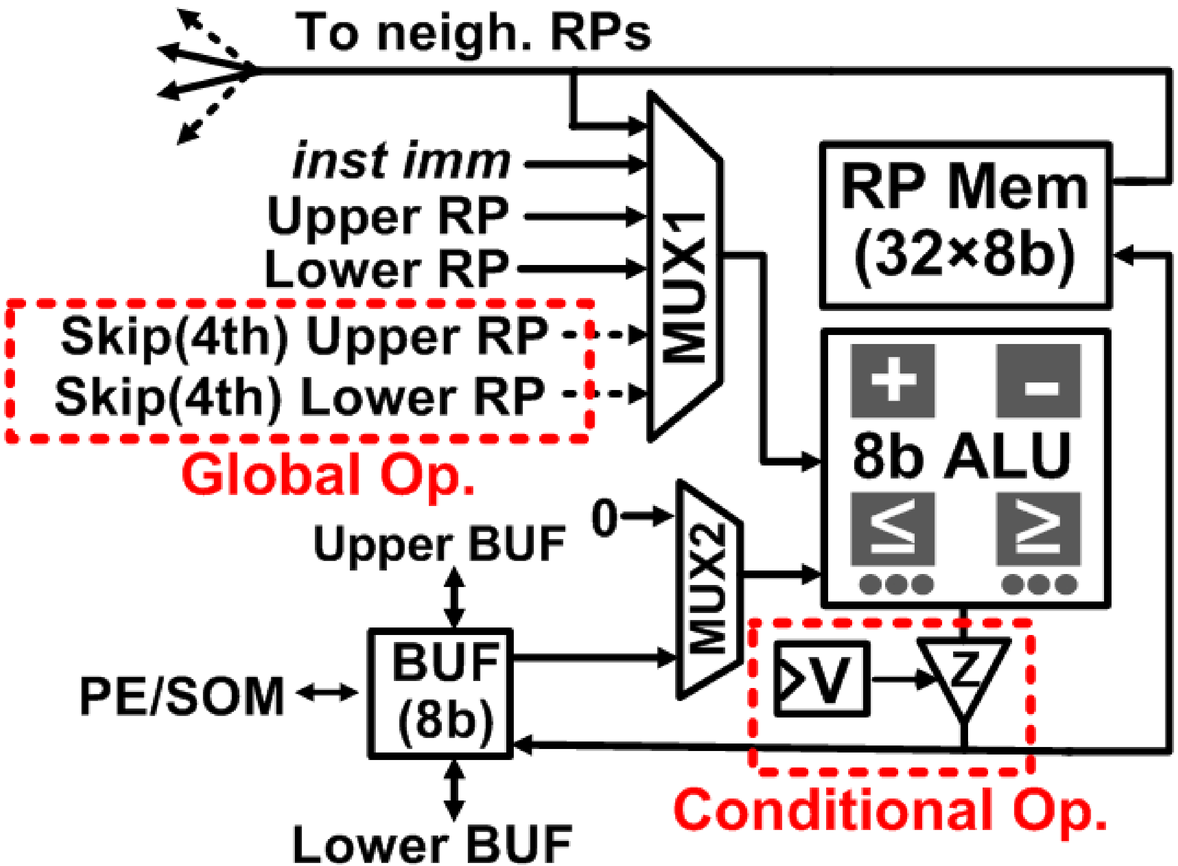
Design of Main Circuits: CG



CG (Conditional Generator) :

- Generate conditional flags for SOM operations.

Design of Main Circuits: RP

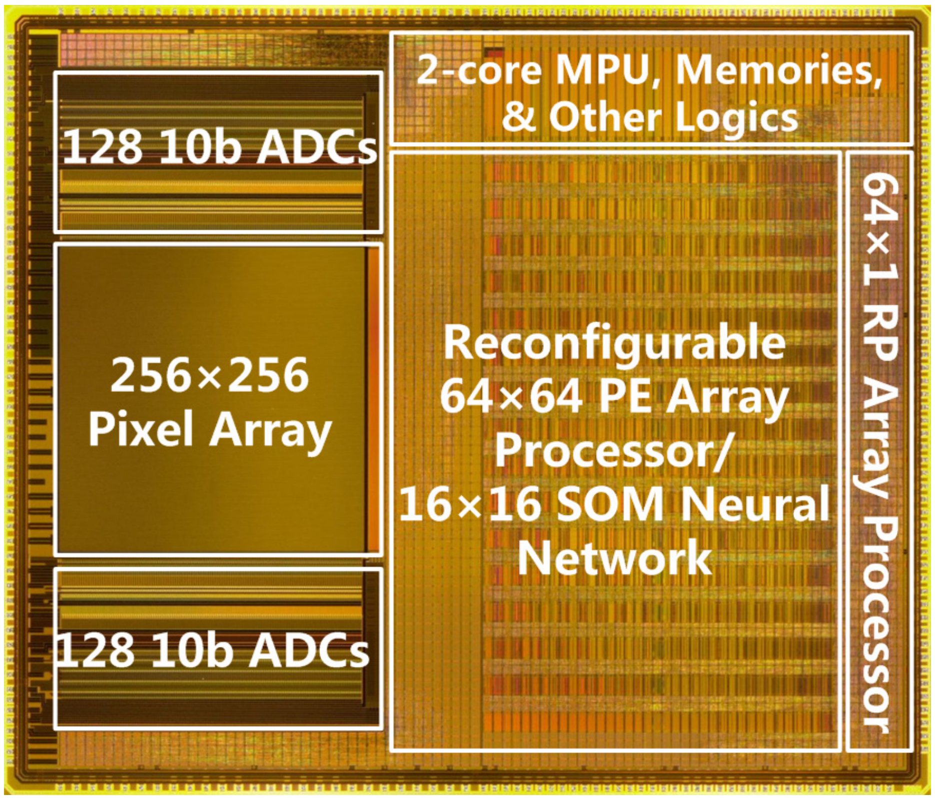


RP (Row Processor) :

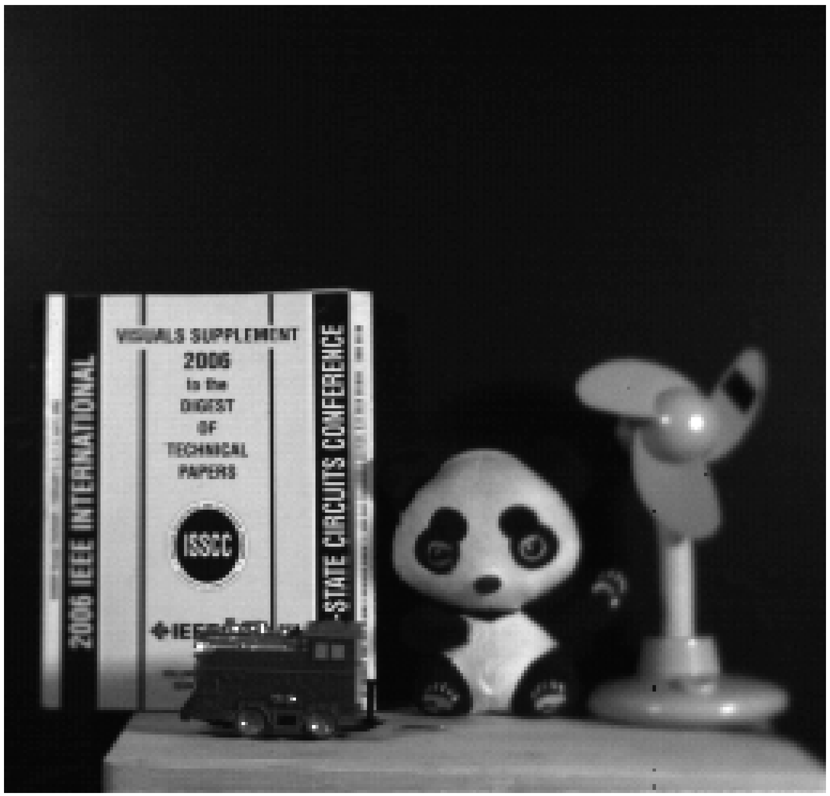
- 8b ALU operation (ADD, SUB, MAX, MIN, SHIFT, …)
- 8b conditional operation
- Fast global operation

Measurement Results

Chip Microphotograph



256×256 Raw Image



@2000fps

Measurement Results

Chip Characteristics

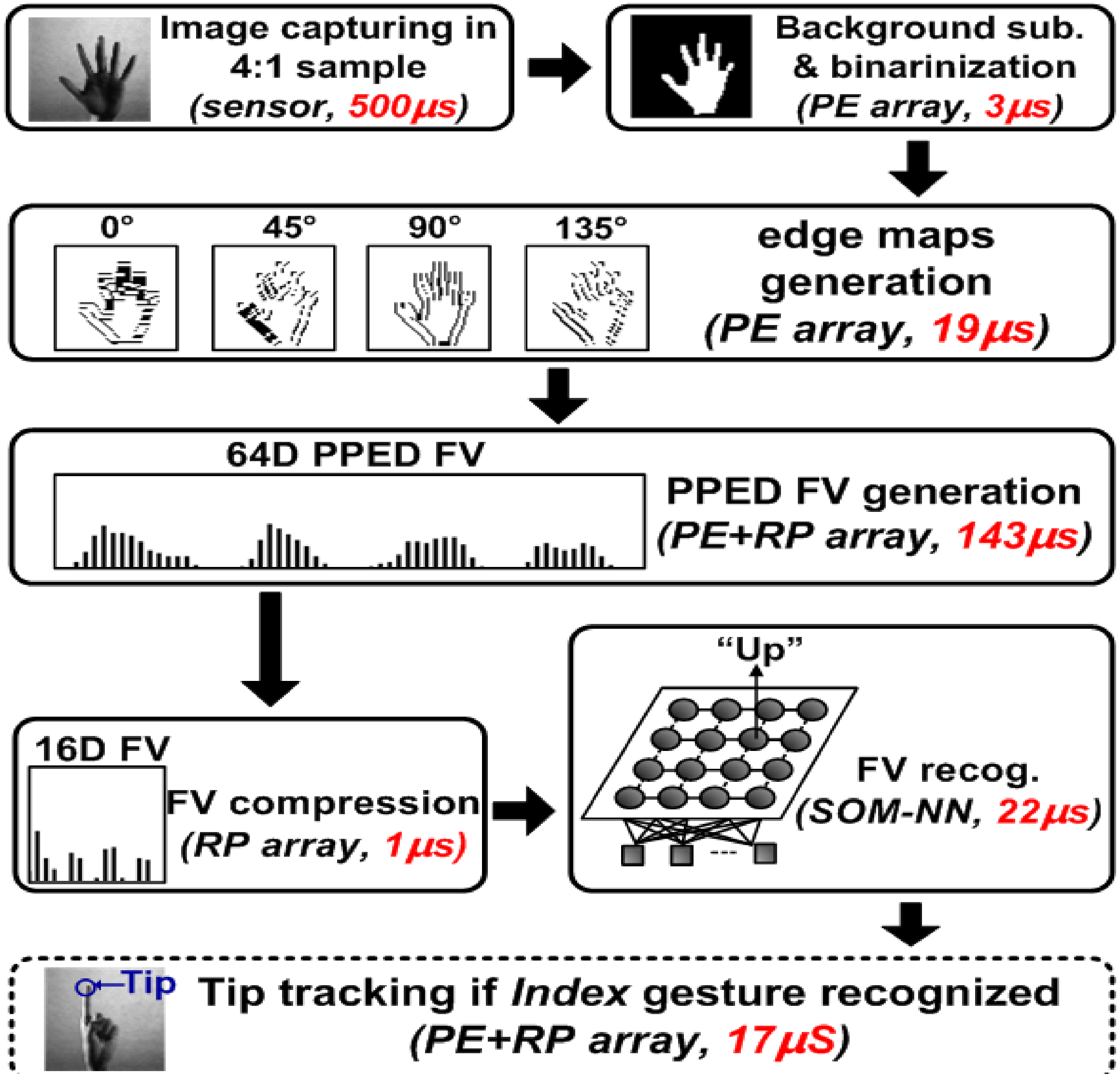
Technology	0.18μm 1P5M CIS
Chip area (pad incl.)	9.8mm×8.4mm
Package	BGA 312pin
Clock frequency	50MHz
Supply voltages	1.8V for digital and ADC 3.3V for I/O and pixel
Power consumption	630mW
Pixel size	10μm×10μm
Pixel fill factor	60%
Pixel sensitivity	8.13V/Lux·s
Pixel DR	48dB

Max. sensor frame rate	1500fps@256×256 3000fps@128×128 6000fps@64×64
Processor performance	PE array processor: 12GOPS @8b gray img 108GOPS @1b binary img RP array processor: 1.6GOPS @8b data Dual-core MPU: ~0.1GOPS @32b data SOM network: 45.4KRPS* @16D vector 31.6KRPS* @32D vector

* KRPS = kilo recognitions per second

Measurement Results

1000fps Hand Gesture Recognition: Algorithm



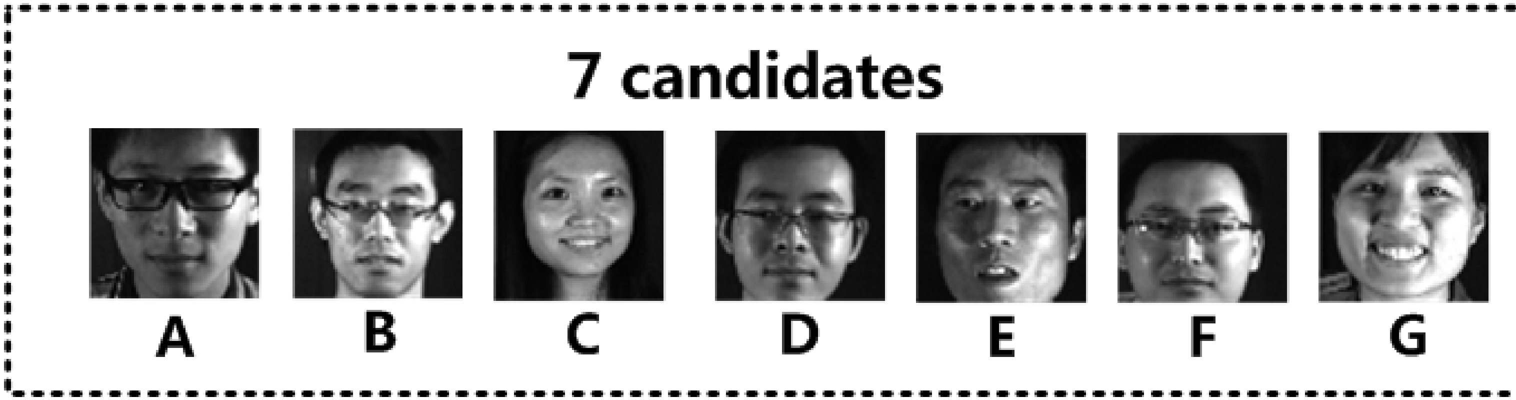
Measurement Results

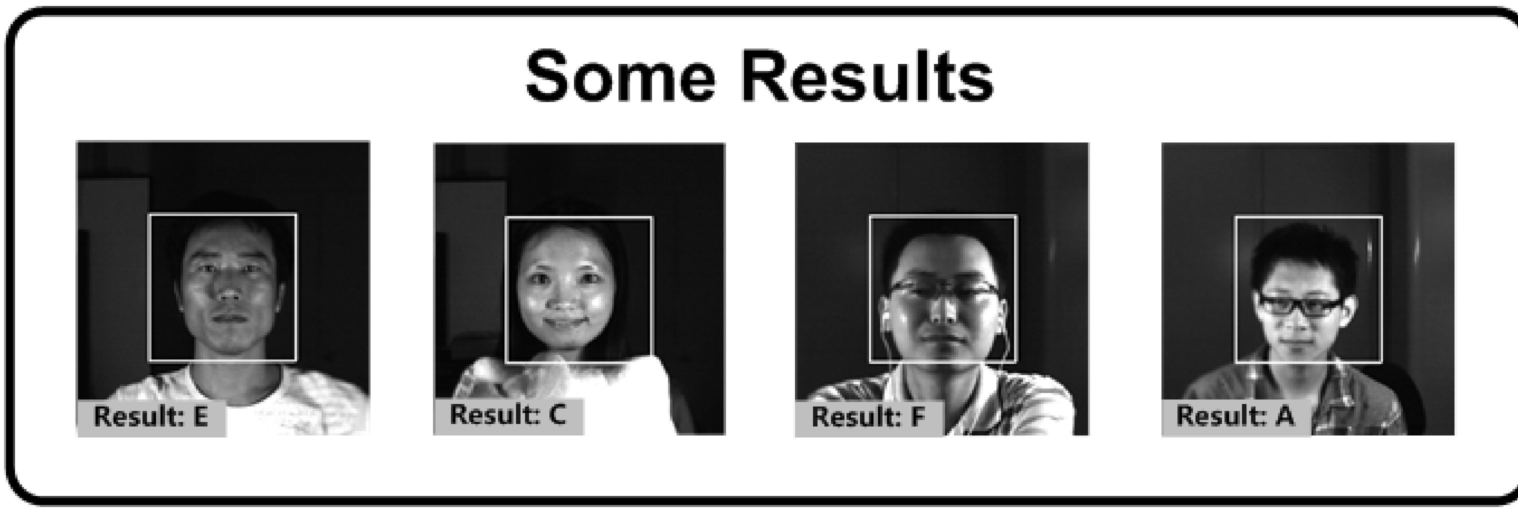
1000fps Hand Gesture Recognition: Results

Grasp Yeah Up Fist Palm Index Down

Measurement Results

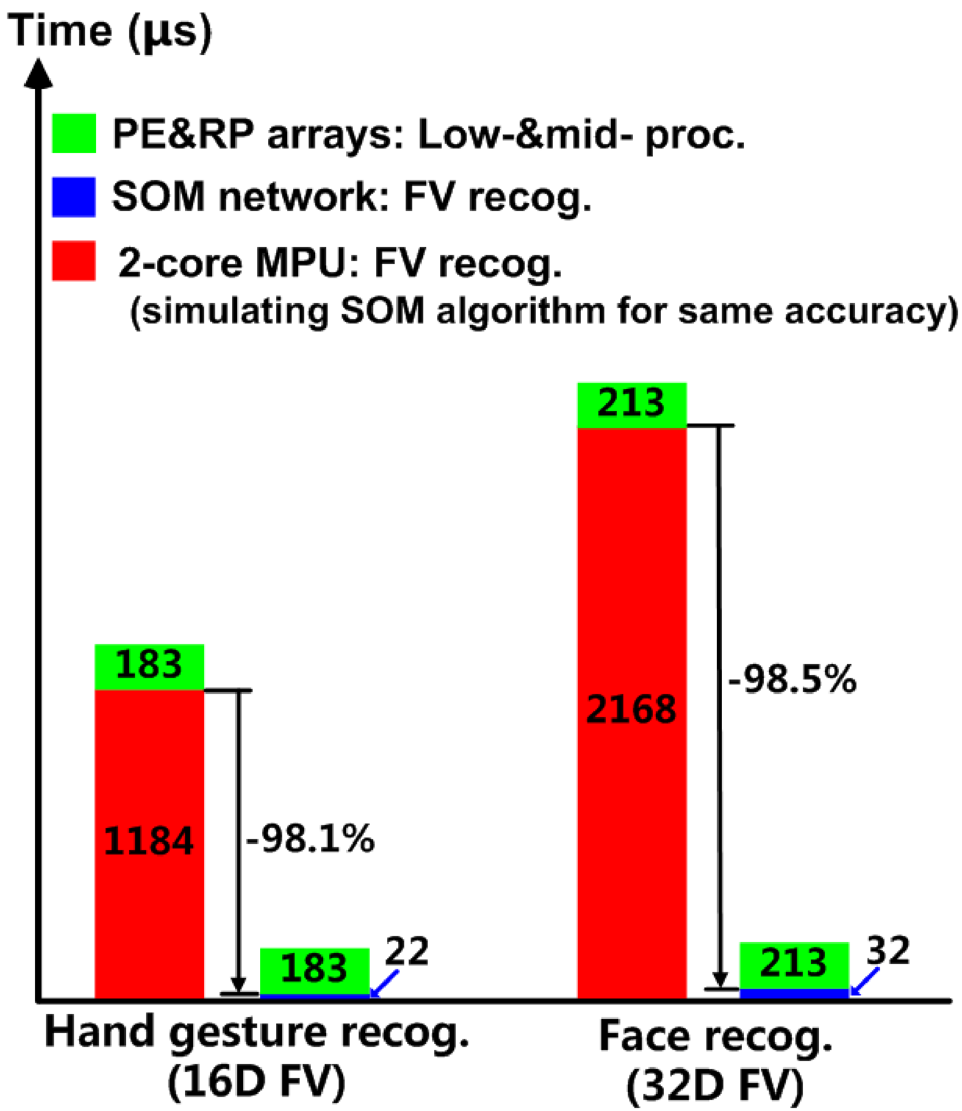
1000fps Face Recognition: Results

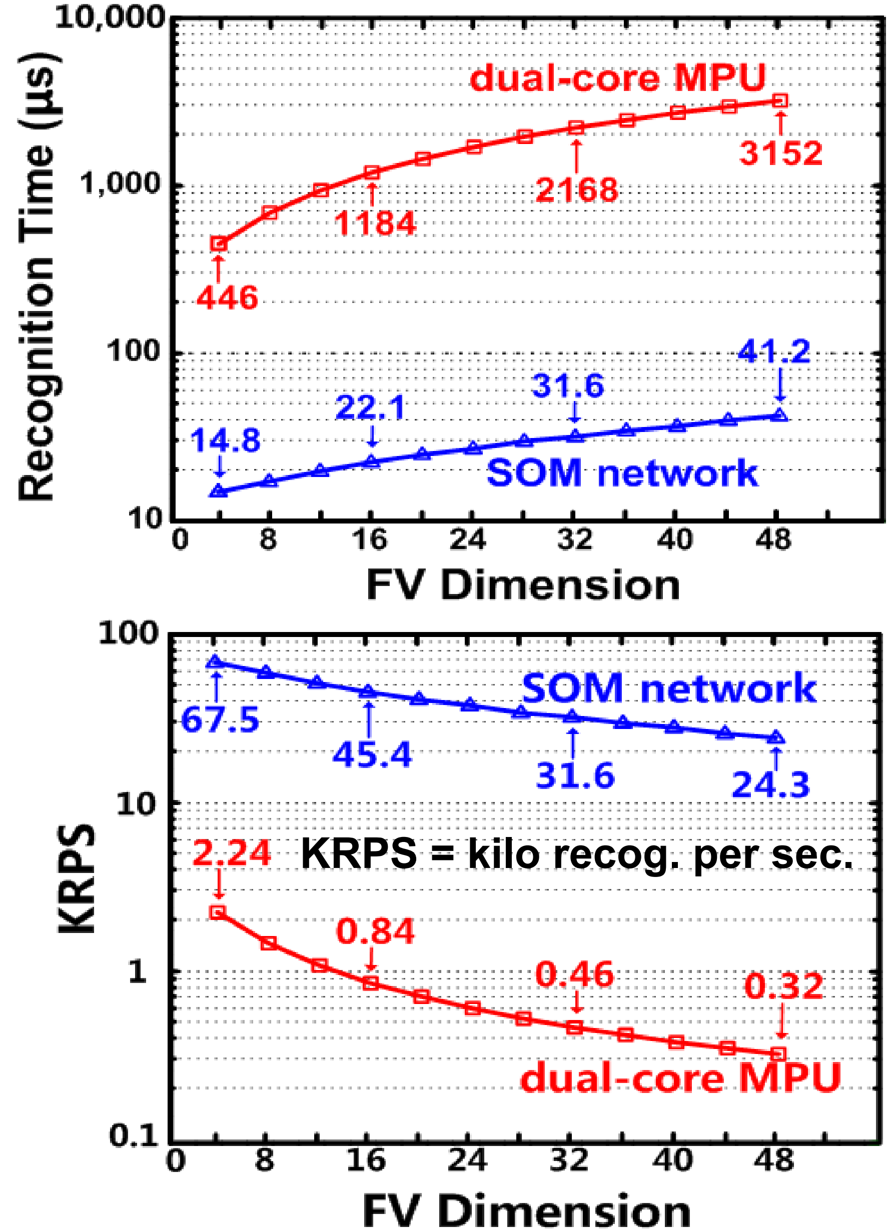




- Using similar algorithm as in hand gesture recognition
- Using 2:1 pixel sample on central 128×128 region
- Extracting 32D PPED vector directly from gray image

Measurement Results: SOM vs. MPU





Comparison Table

	This work	W. Miao, et al. [JSSC2008]	W. Jendernalik, et al. [TCAS2013]	C. Cheng, et al. [ISSCC2008]	W. Zhang, et al. [JSSC2011]
Technology	0.18μm 1P5M	0.18μm 1P6M	0.35μm 2P4M	0.18μm 2P4M	0.18μm 1P6M
Area	82.3 mm^2	2.3 mm^2	9.8 mm^2	70.5 mm^2	13.5 mm^2
Power	630 mW	8.72 mW	0.28 mW	455 mW	450 mW
Clock	50 MHz	20 MHz	N/A	50 MHz	100 MHz
Sensor resolution	256×256	16×16	64×64	128×128	128×128
Pixel fill factor	60%	3%	23%	N/A	58%
Parallelism	Pixel-, row-, thread-, vector-	Pixel-, row-	Pixel-	Row-	Pixel-, row-
Reconfigurability	Dynamic (PE array / SOM network)	No	No	No	Static (different PE array sizes)
High-level processors	SOM network, 2-core MPU	No	No	1-core MPU	1-core MPU
Low-,mid-levels performance	12 GOPS	0.2 GOPS	0.1ms, 3x3conv. (~0.45 GOPS)	76.8 GOPS	44 GOPS
High-level performance	45.4 KRPS[1]@16D 31.6 KRPS@32D	0	0	1.24 KRPS@16D 0.60 KRPS@32D	0.16 KRPS@16D 0.08 KRPS@32D
System performance	1340 fps (face recog.)	N/A	N/A	360 fps (posture recog.)	76 fps (face recog.)
FOM[2] (with 16D FV)	0.1834	~0	~0	0.0380	0.0273
FOM (with 32D FV)	0.1675	~0	~0	0.0192	0.0137

[1]KRPS = kilo recognitions per second.

[2]FOM = $(GOPS^{-1}+KRPS^{-1})^{-1}/Area(mm^2)\cdot Power(W)$.

Summary

- **Hybrid vision chip architecture with both von Neumann processors and non-von Neumann SOM neural network**
- **Multiple levels of parallelism: pixel-, row-, vector-, thread-parallelism**
- **Dynamic reconfiguration between PE array processor and SOM network**
- **1000 fps system-level performance from image capture to high-level processing**

A 413×240-Pixel Sub-Centimeter Resolution Time-of-Flight CMOS Image Sensor with In-Pixel Background Canceling Using Lateral-Electric-Field Charge Modulators

Sang-Man Han[1], Taishi Takasawa[1], Tomoyuki Akahori[2], Keita Yasutomi[1], Keiichiro Kagawa[1], Shoji Kawahito[1,2]

[1]Shizuoka University, Hamamatsu, Japan
[2]Brookman Technology, Hamamatsu, Japan

Motivation

Application of ToF sensor

Gaming, 3D mice,
Gesture sensor, robots,
Security systems,
automobiles

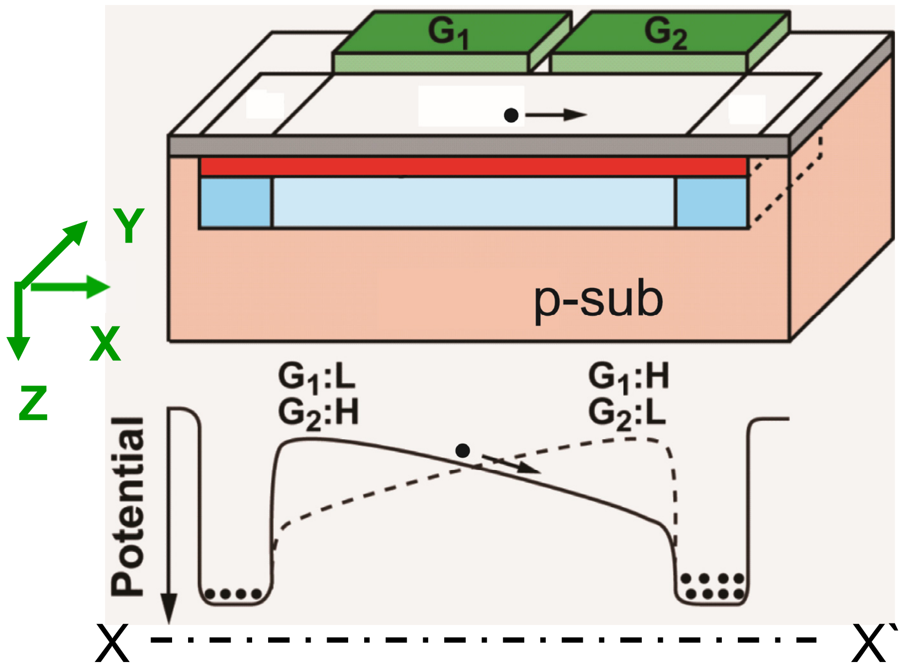
Challenge:
High resolution
- High modulation ratio
- High modulation speed or Short-duration light pulses

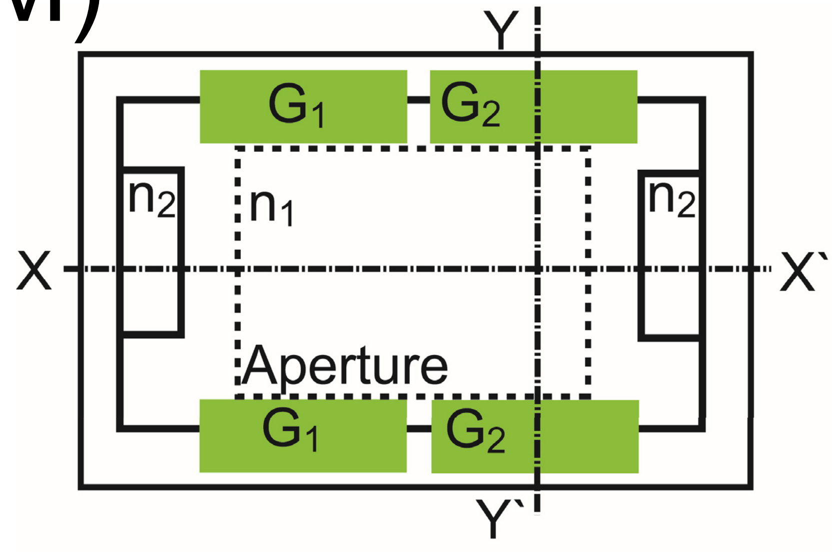
Background-cancelled range image for moving objects
- Multiple-tap charge modulator

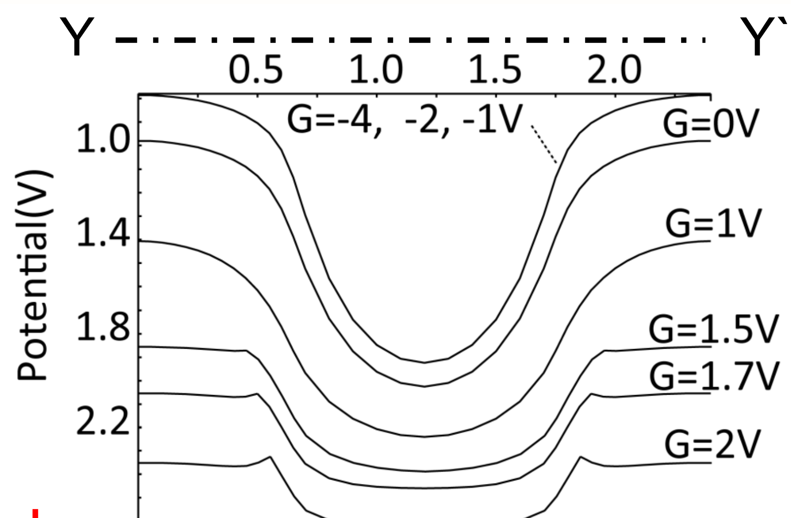
A ToF Range imager using multi-tap Lateral-Electric-Field charge Modulators (LEFM)

Lateral-electric-field charge modulators (LEFM)

Two-tap LEFM [8]







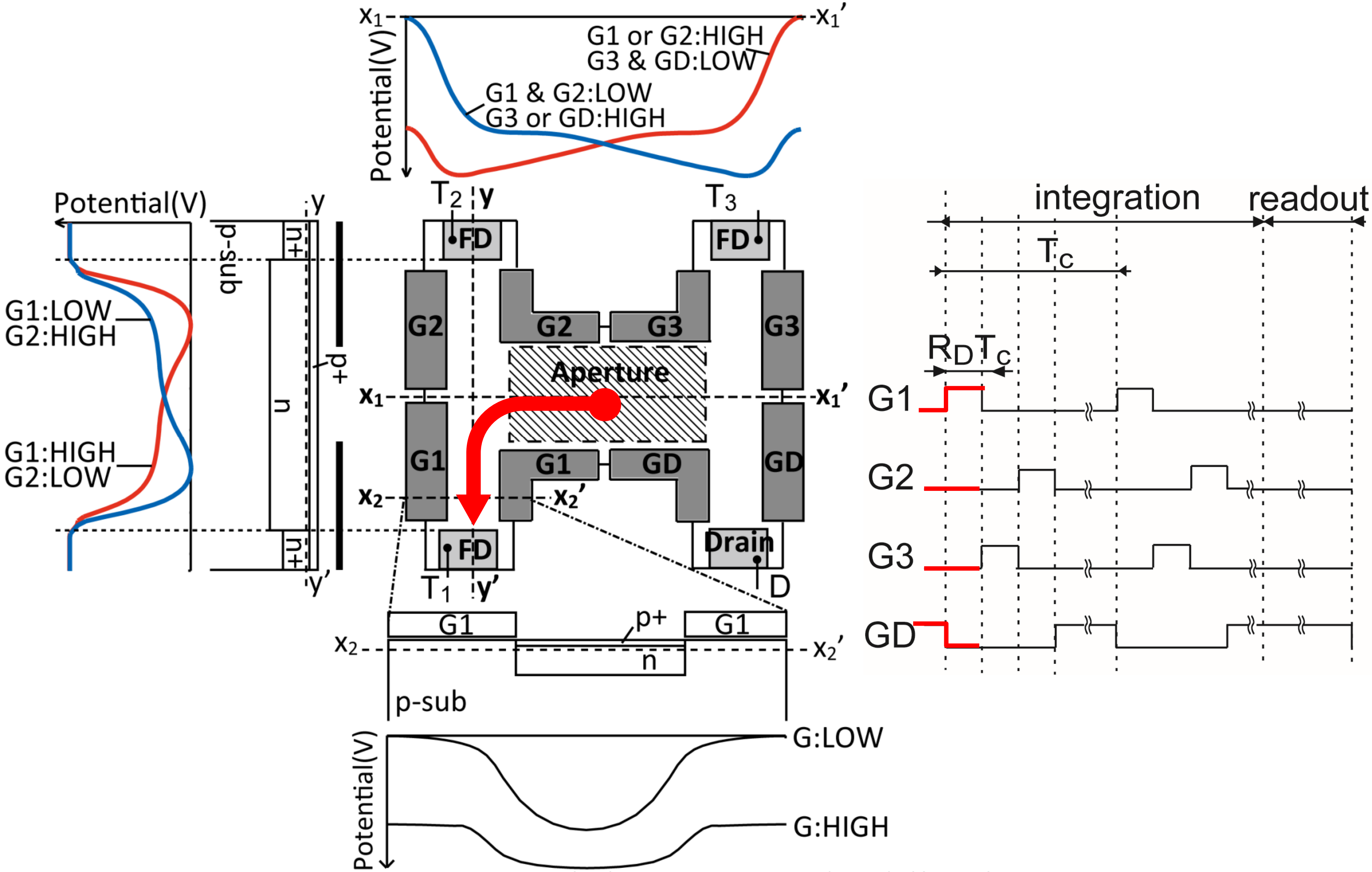
Lateral-electric-field charge modulators (LEFM)

- High-speed charge transfer
- Easy to implement **multiple taps**

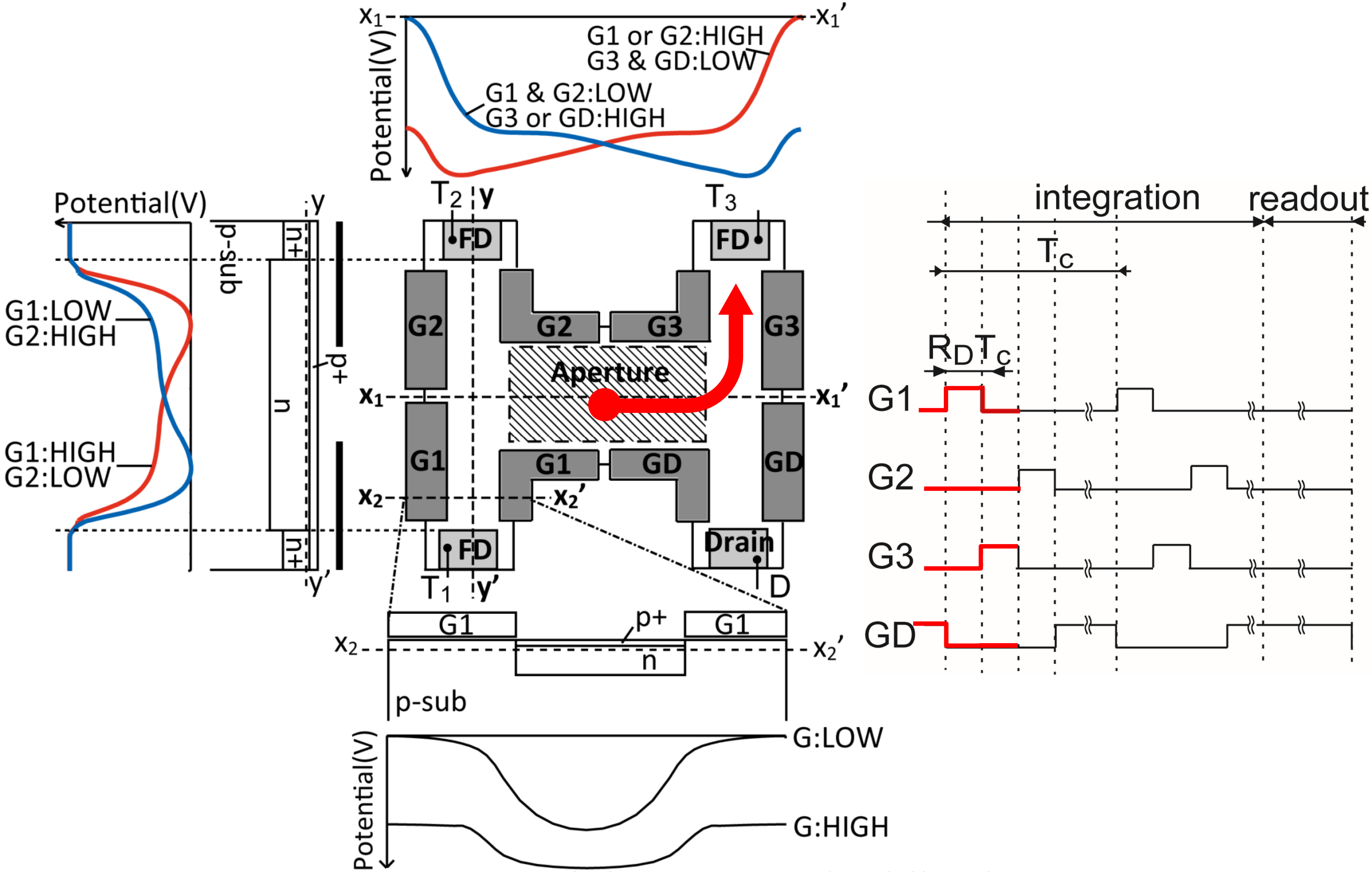
➢ToF sensor with in-pixel background light canceling for moving object

[8] S. Kawahito, et al. IISW 2013

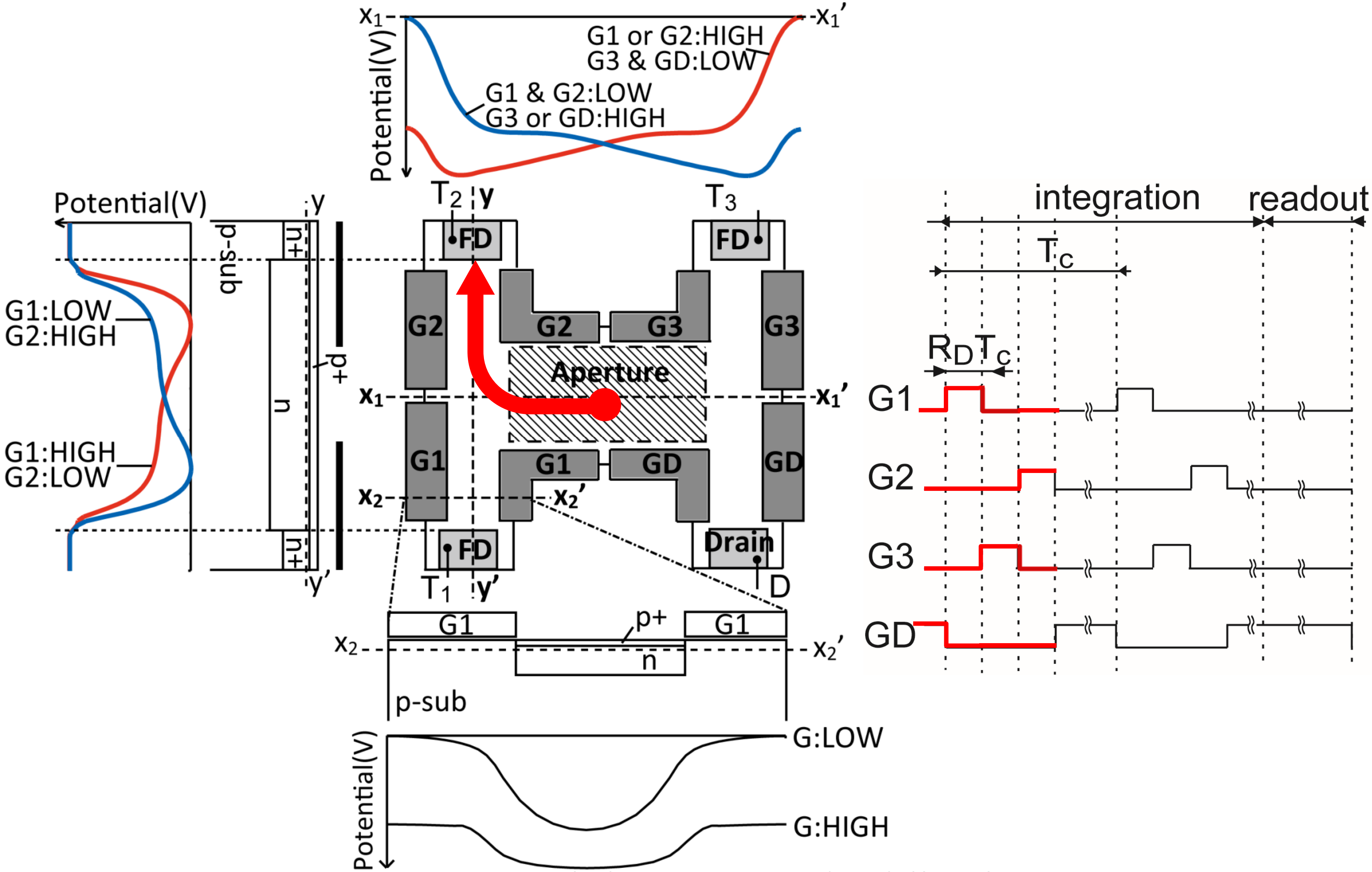
Charge modulator architecture



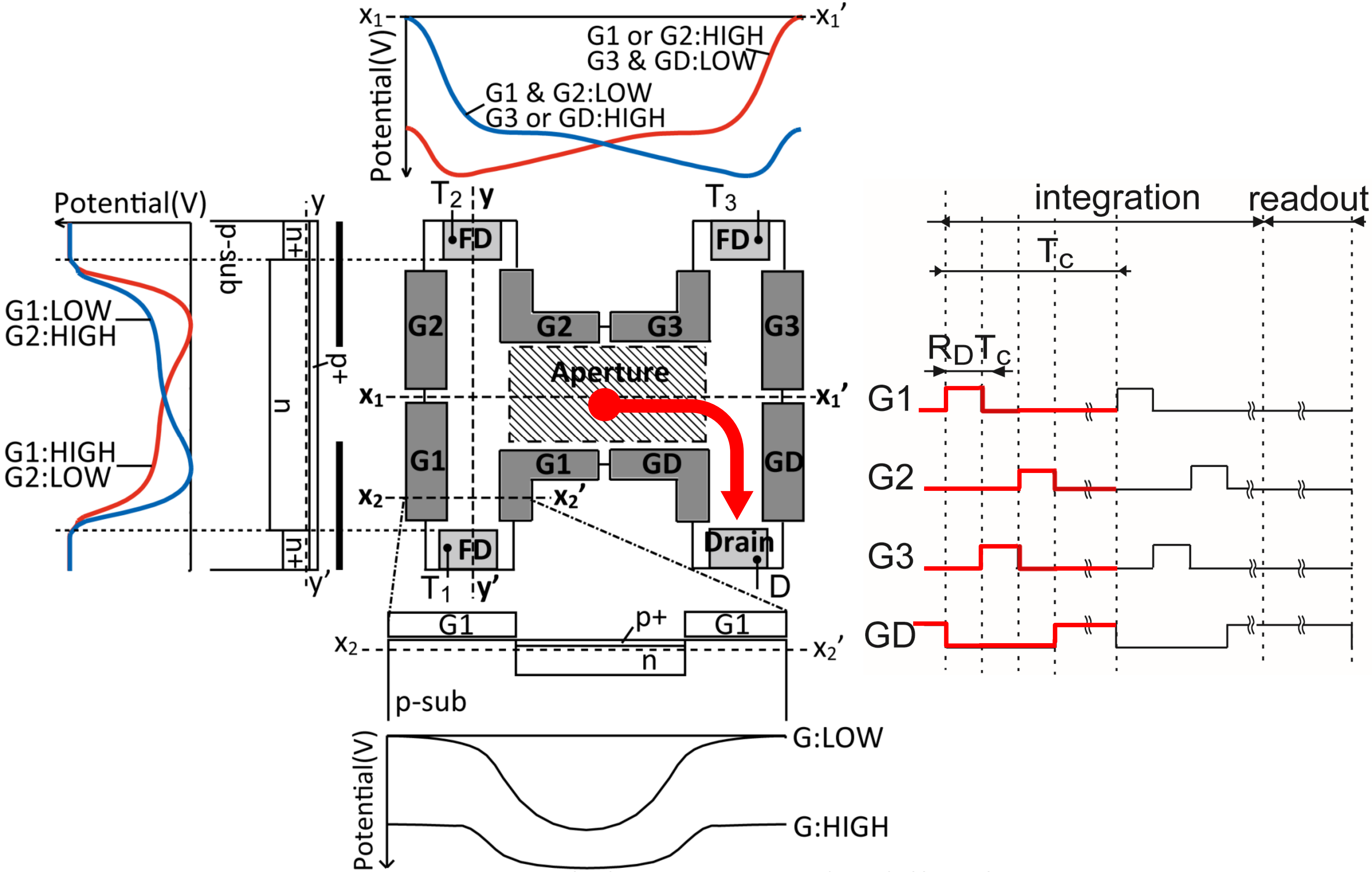
Charge modulator architecture



Charge modulator architecture

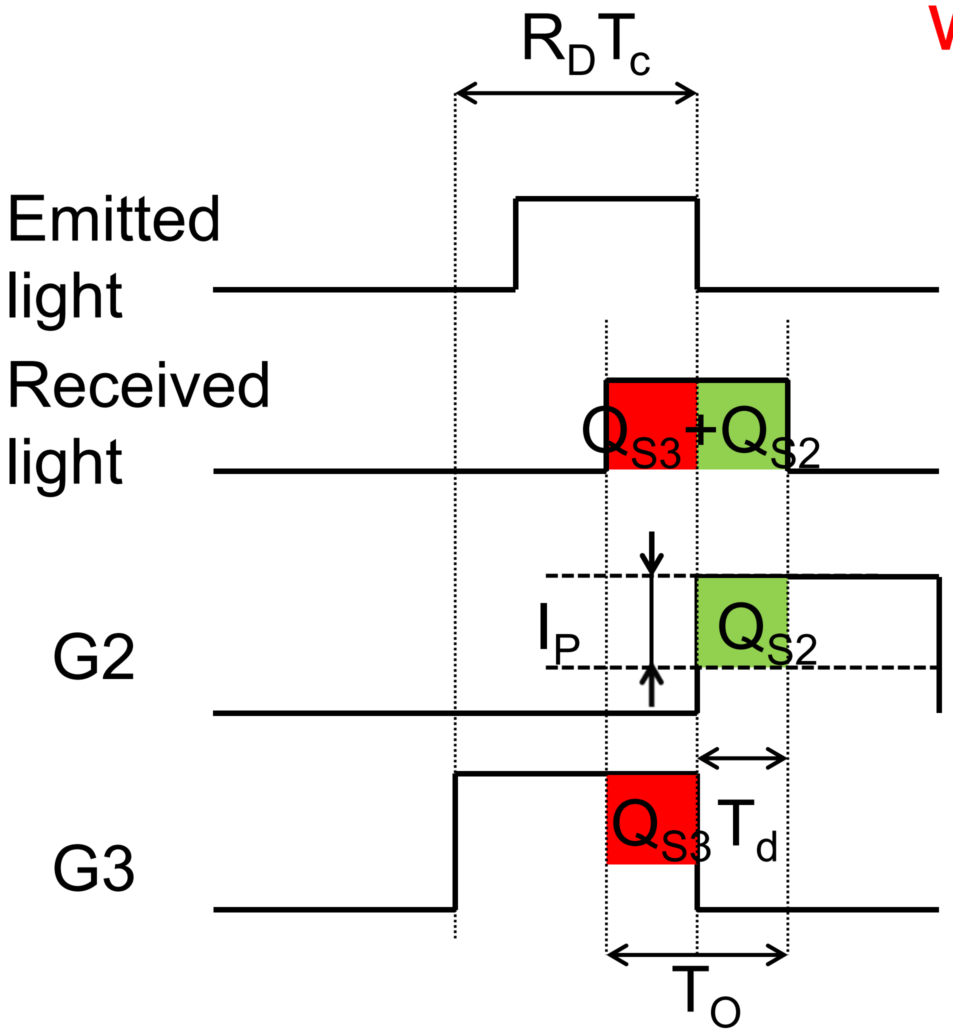


Charge modulator architecture



Background light canceling

w/o background light



$$Q_2 = Q_{S2} = I_P T_d$$

$$Q_3 = Q_{S3} = I_P (T_O - T_d)$$

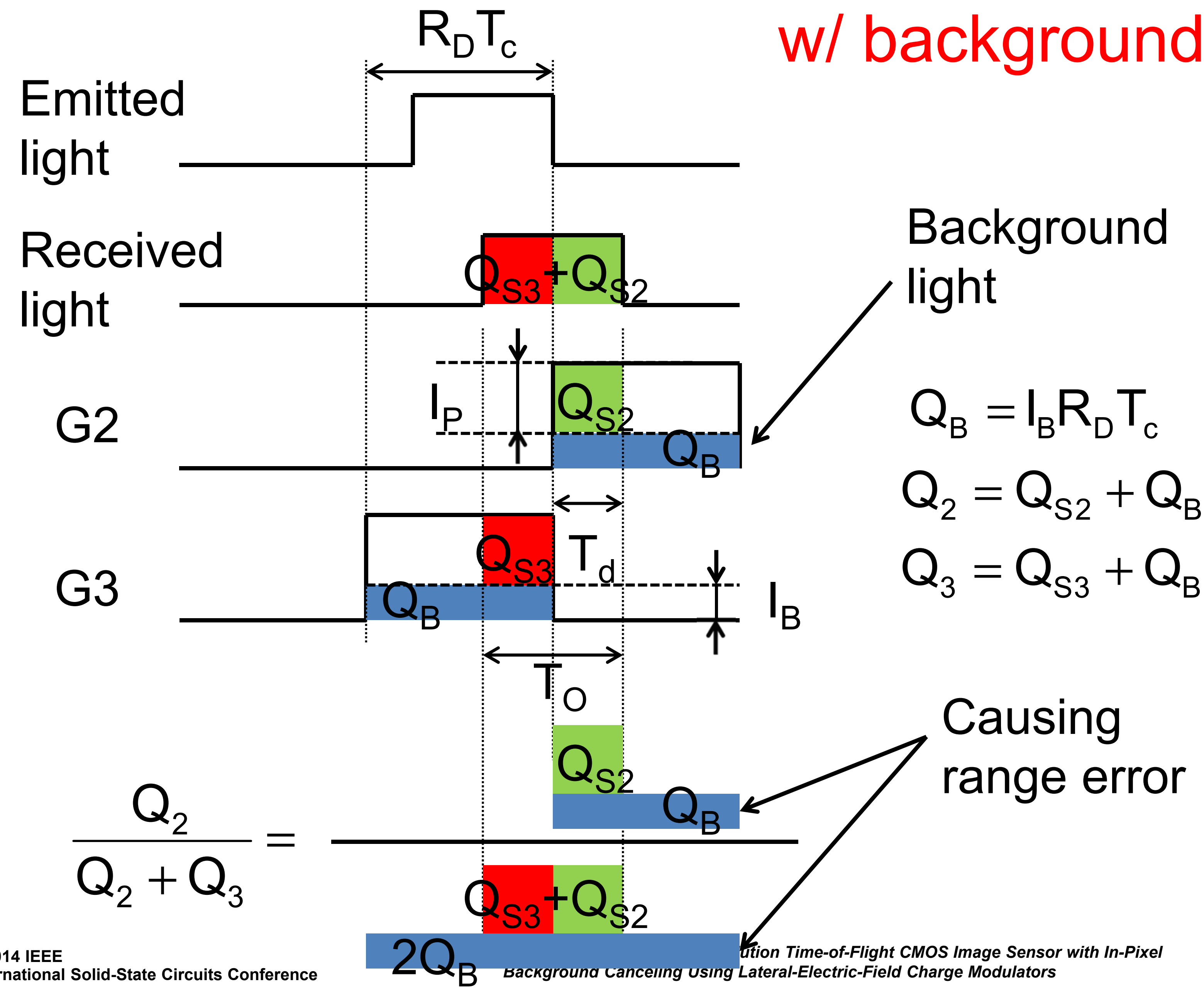
$$T_d = T_O \left(\frac{Q_2}{Q_2 + Q_3} \right)$$

$$L = \frac{c}{2} T_d$$

$$= \frac{c}{2} T_O \left(\frac{Q_2}{Q_2 + Q_3} \right)$$

Background light canceling

w/ background light



$$\frac{Q_2}{Q_2+Q_3}=$$

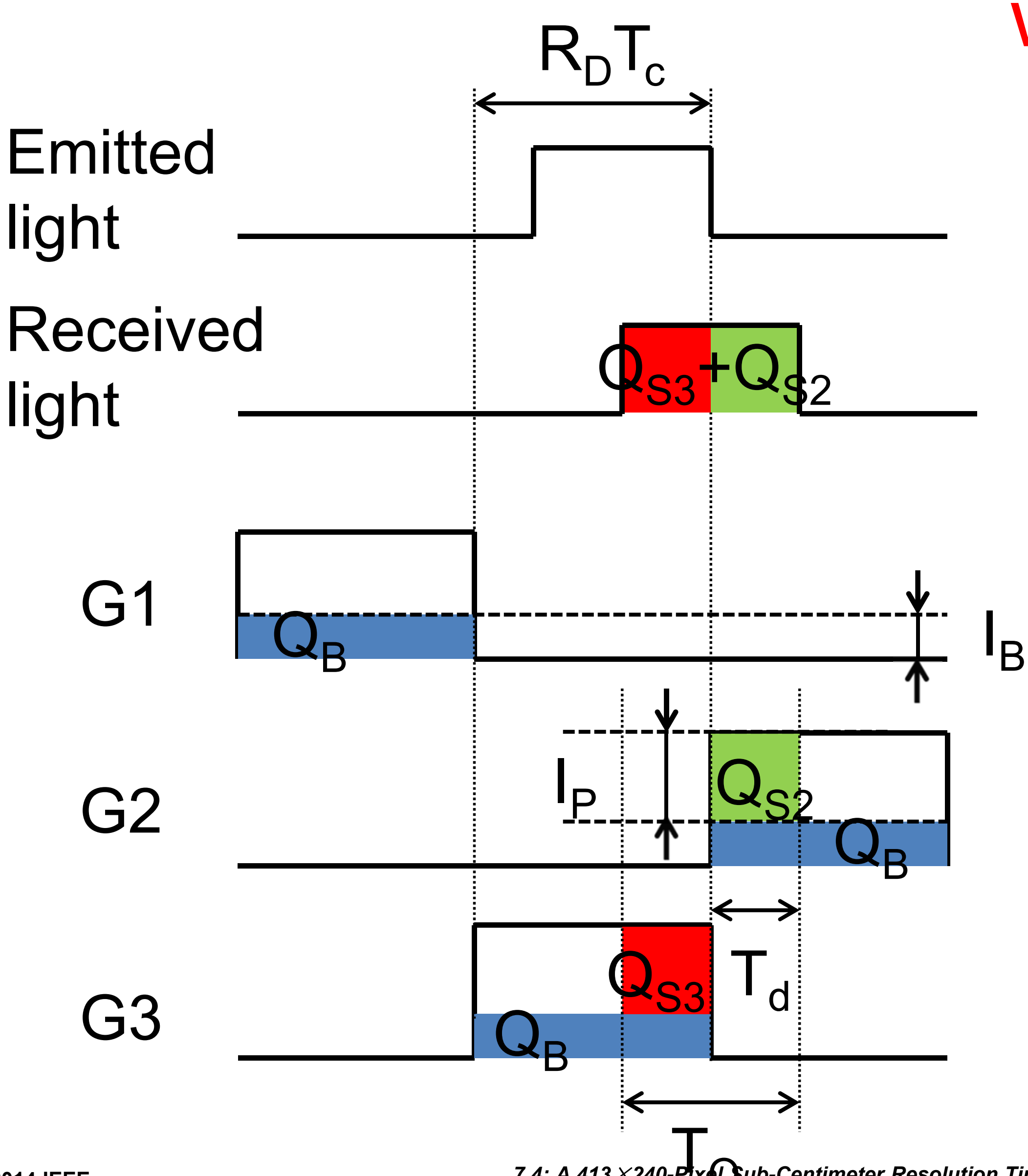
$$Q_B = I_B R_D T_c$$

$$Q_2 = Q_{S2} + Q_B$$

$$Q_3 = Q_{S3} + Q_B$$

Background light canceling

w/ background Light



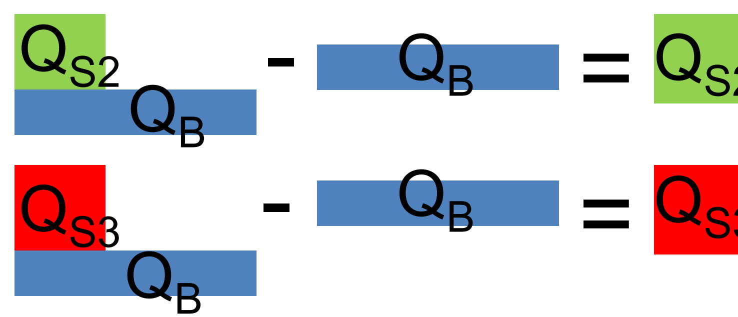
$$Q_1 = I_B R_D T_c = Q_B$$

$$Q_2 = Q_{S2} + Q_1$$

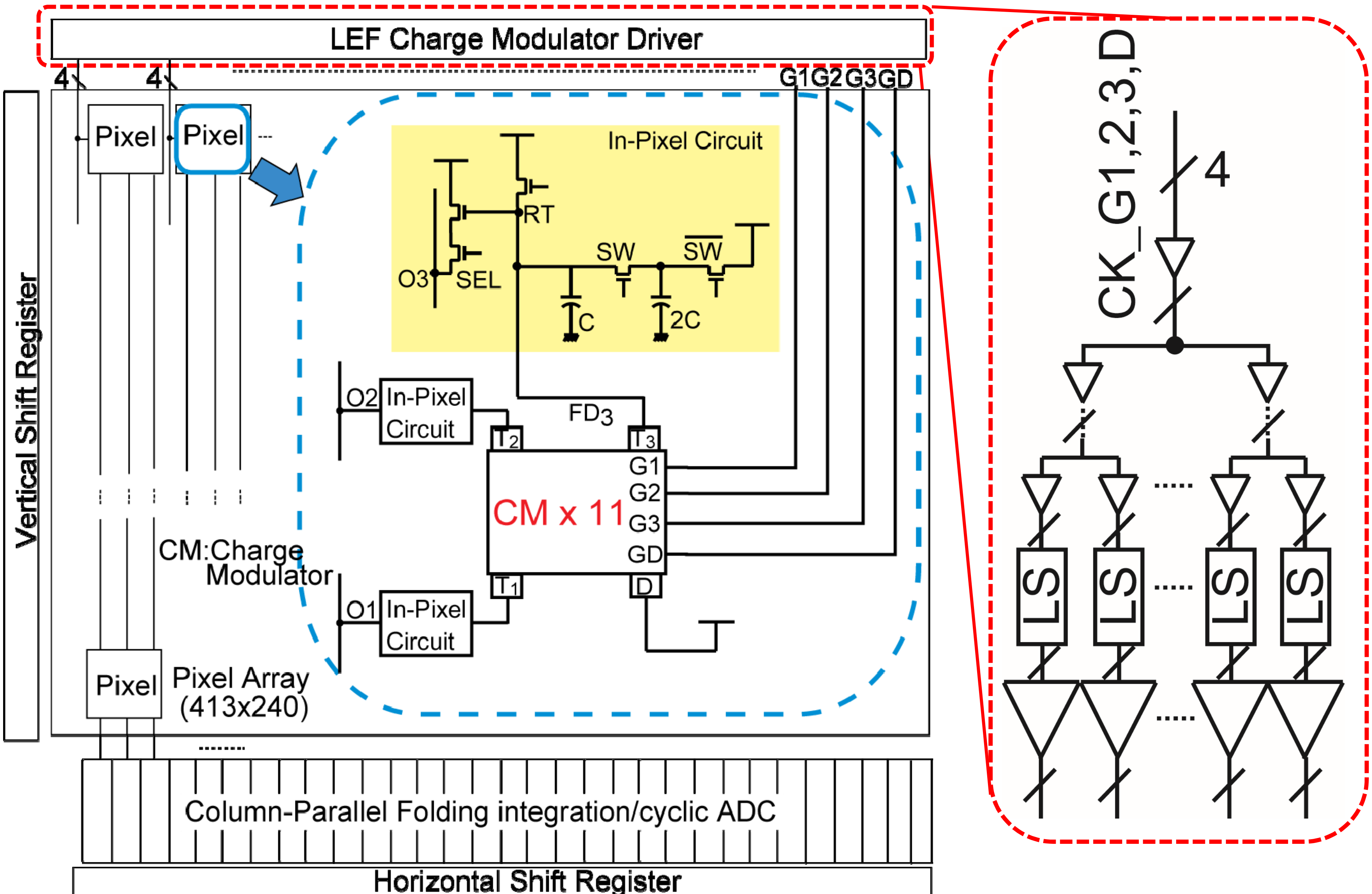
$$Q_3 = Q_{S3} + Q_1$$

$$L = \frac{c}{2} T_d$$

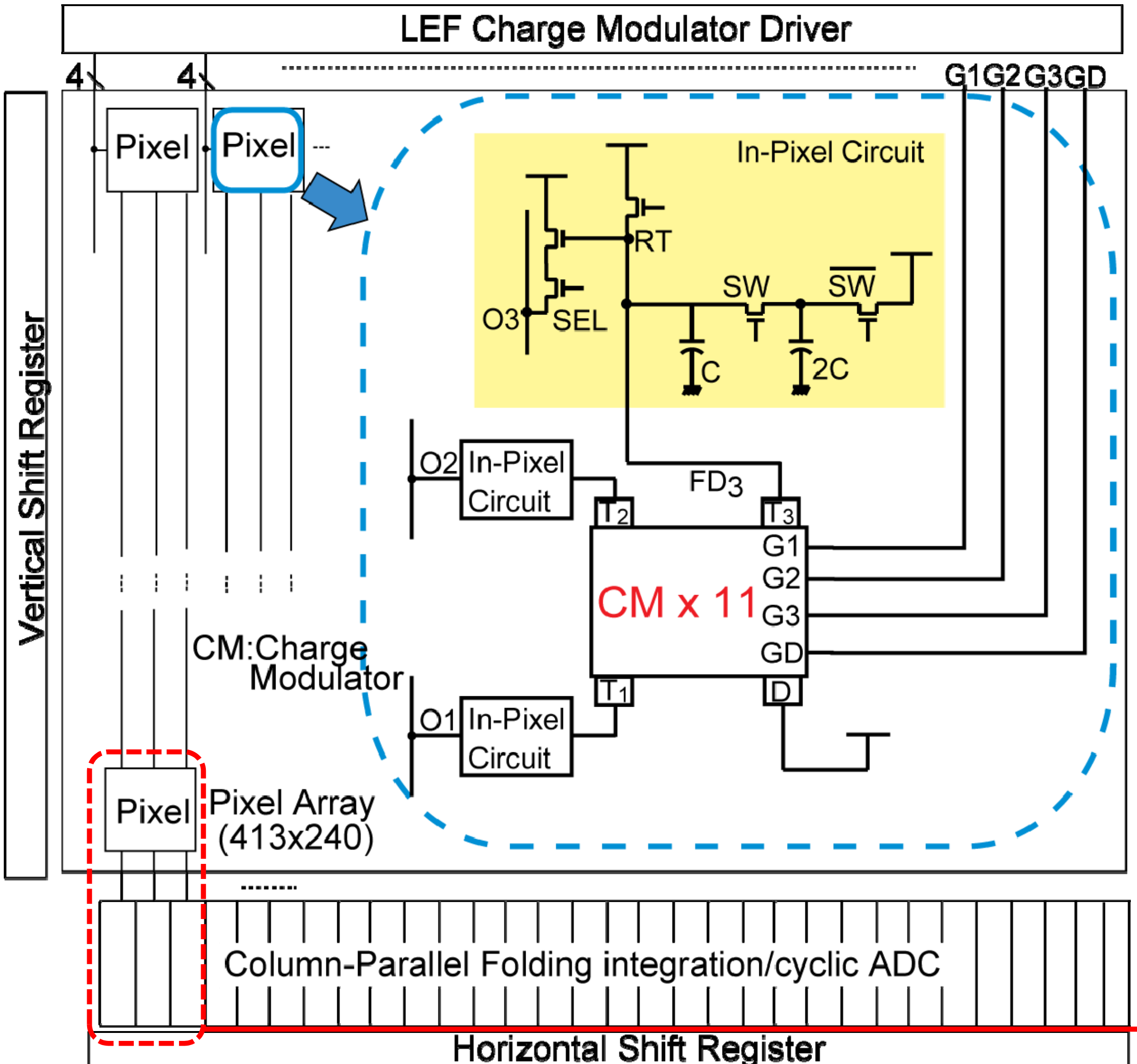
$$= \frac{c}{2} T_O \left(\frac{Q_2 - Q_1}{Q_2 + Q_3 - 2Q_1} \right)$$



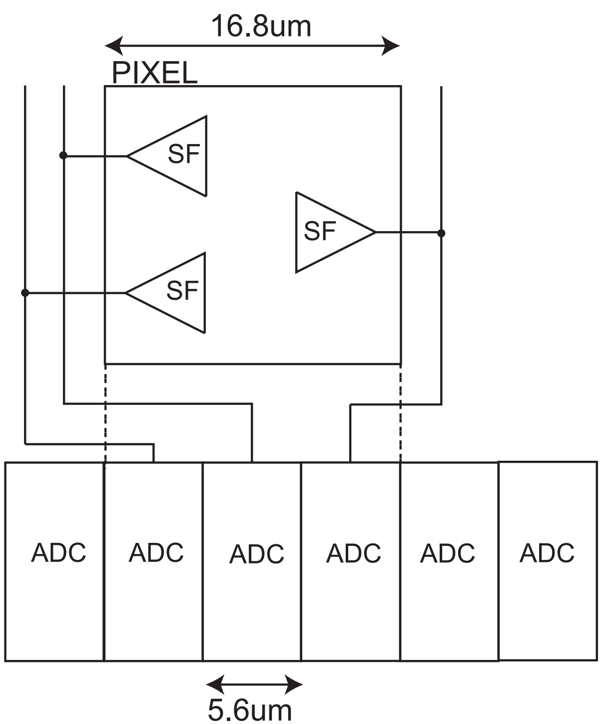
Chip architecture



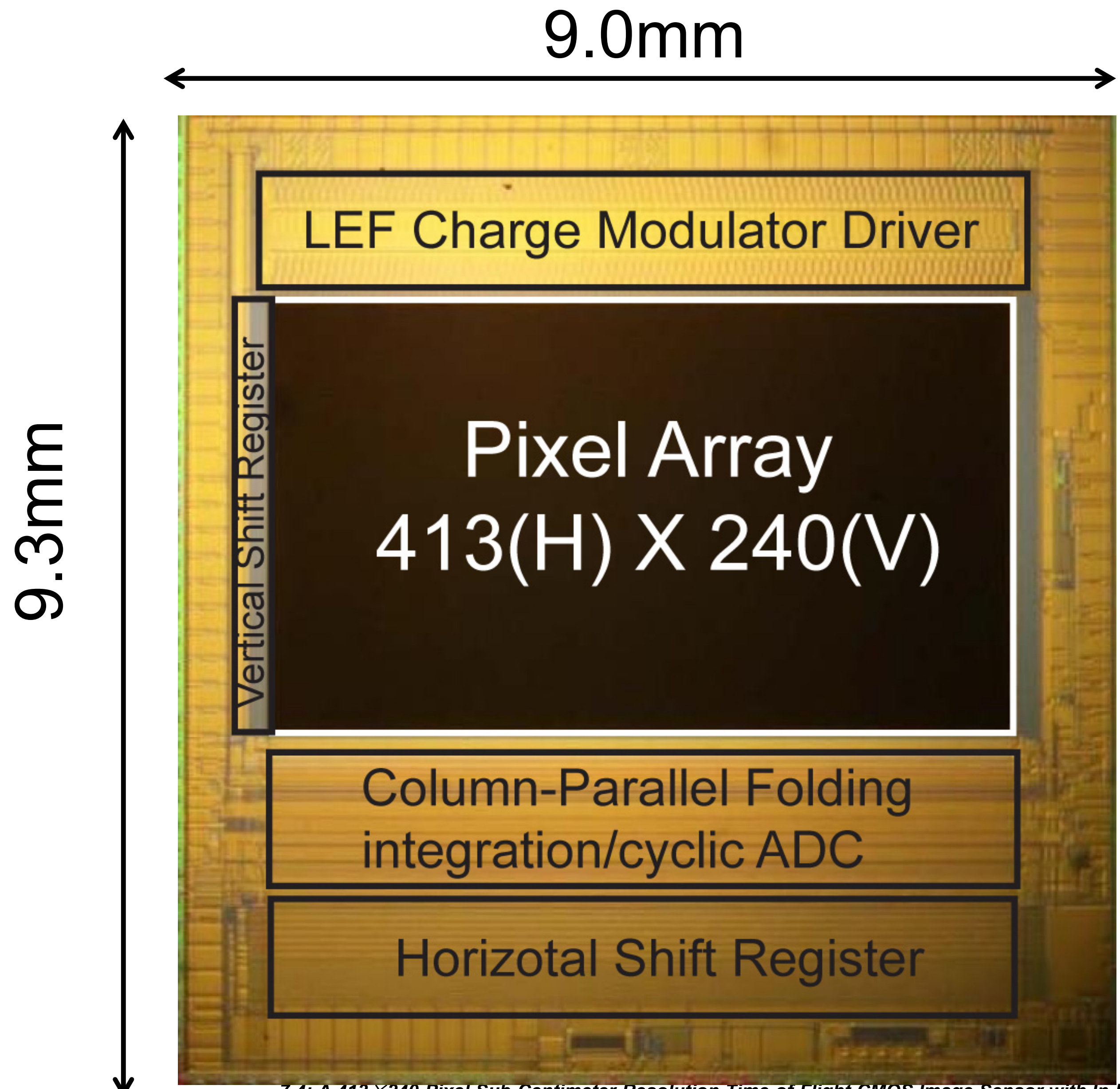
Chip architecture



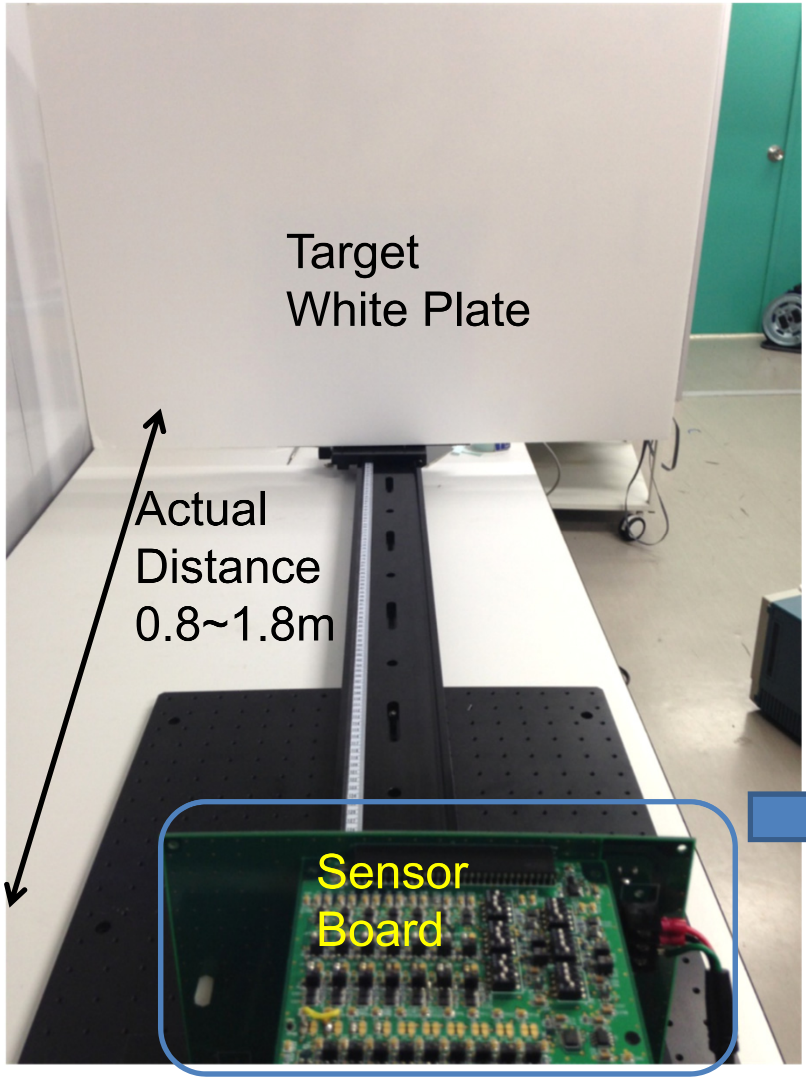
1 Pixel pitch =
3 Column ADC pitch



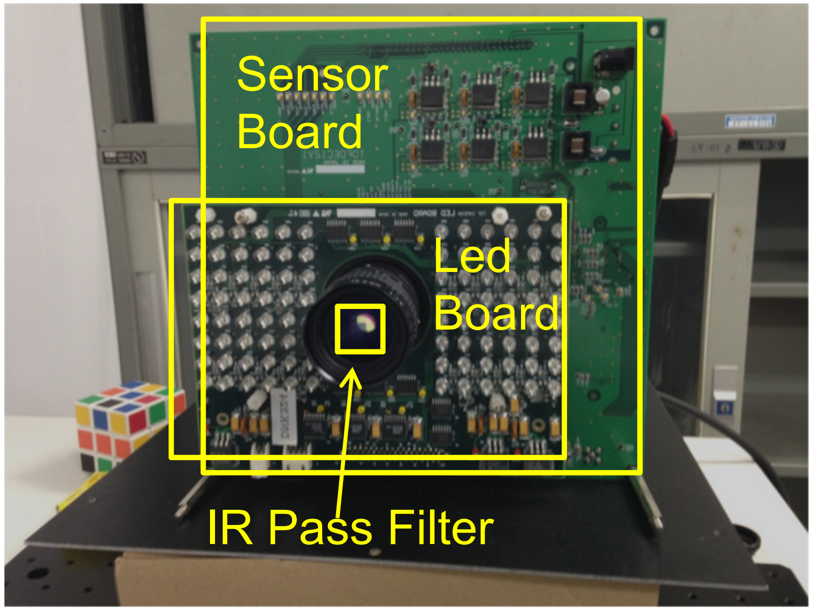
Chip photomicrograph



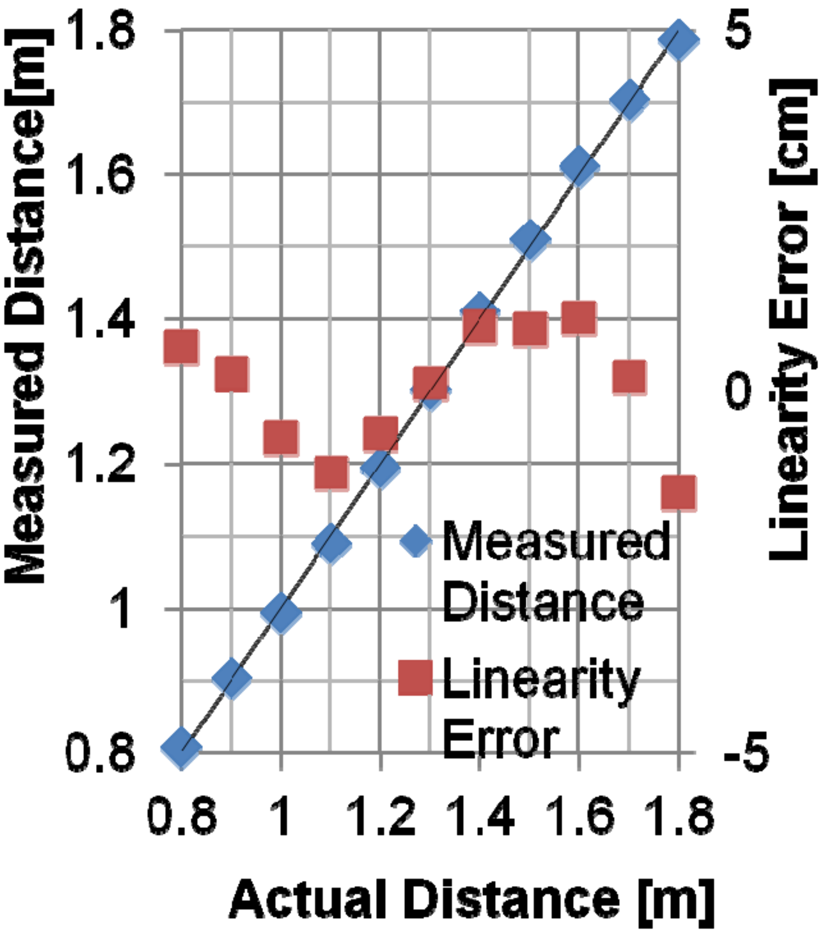
Measurement system

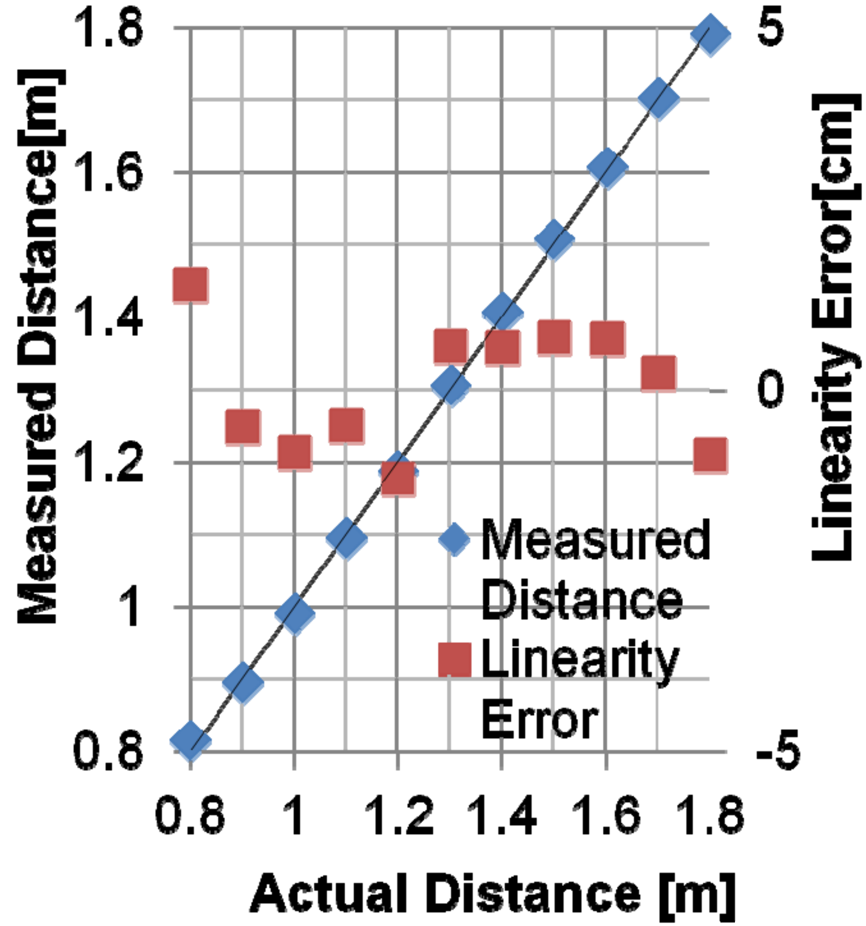


Number of LED : 96
Average LED Power : 250 mW
Wavelength : 870nm
Band pass width of IR filter : 40nm



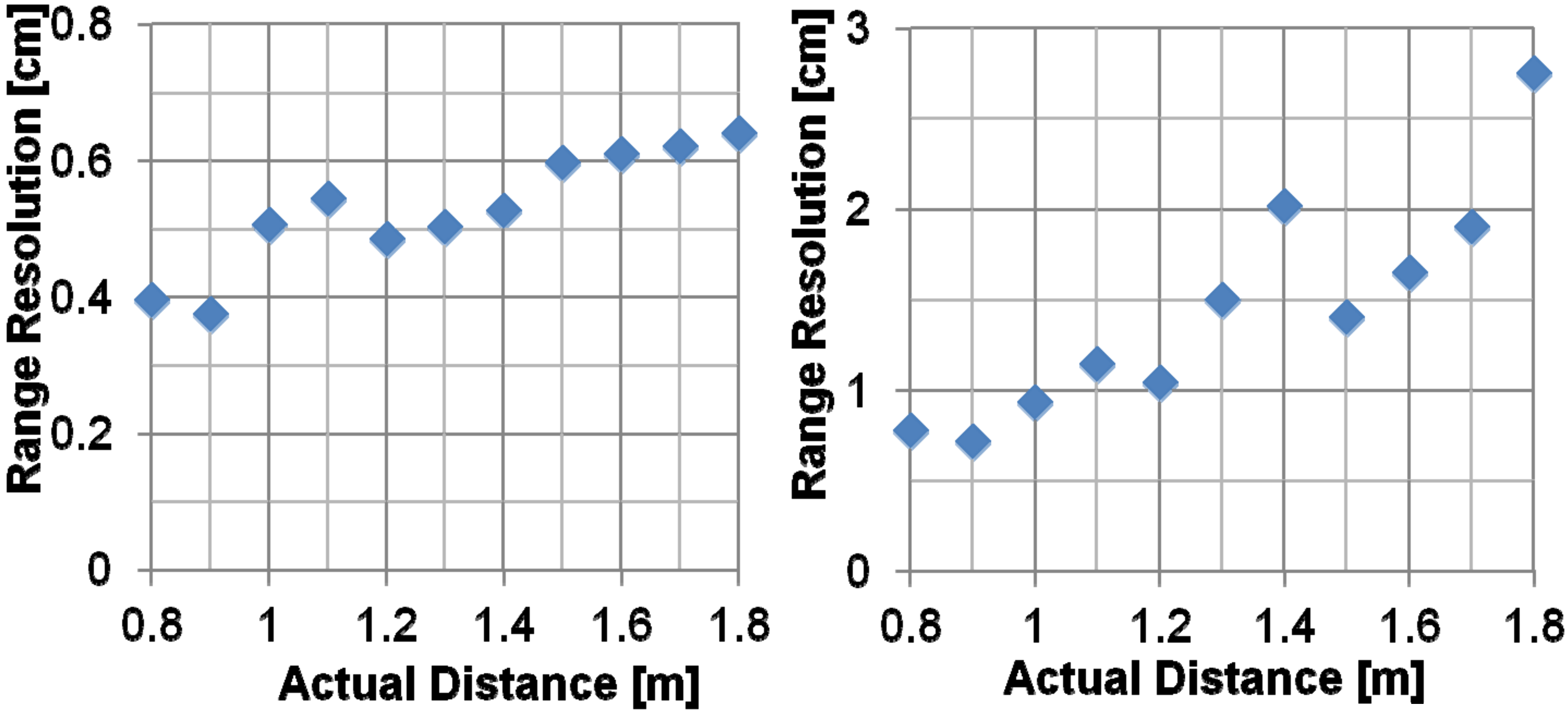
Range linearity w (right) & w/o (left) background light





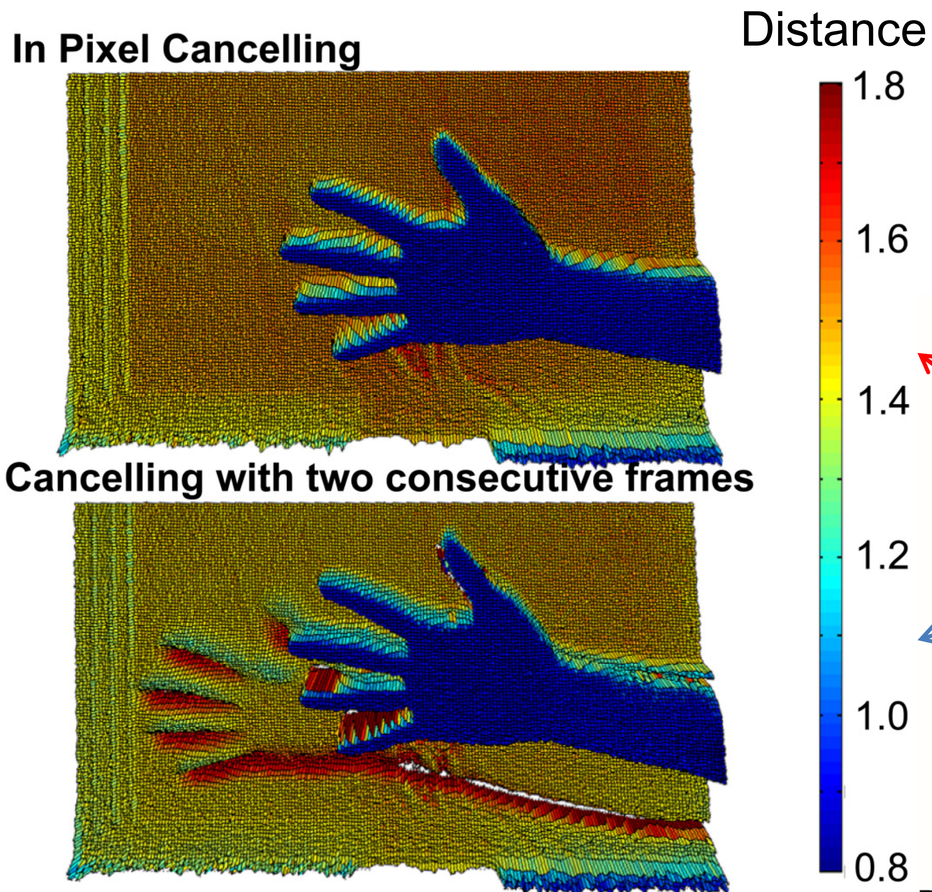
The depth data of 30 frames of 10x10 pixels in the center of the array captured by 15fps are averaged

Range resolution w (right) & w/o (left) background light

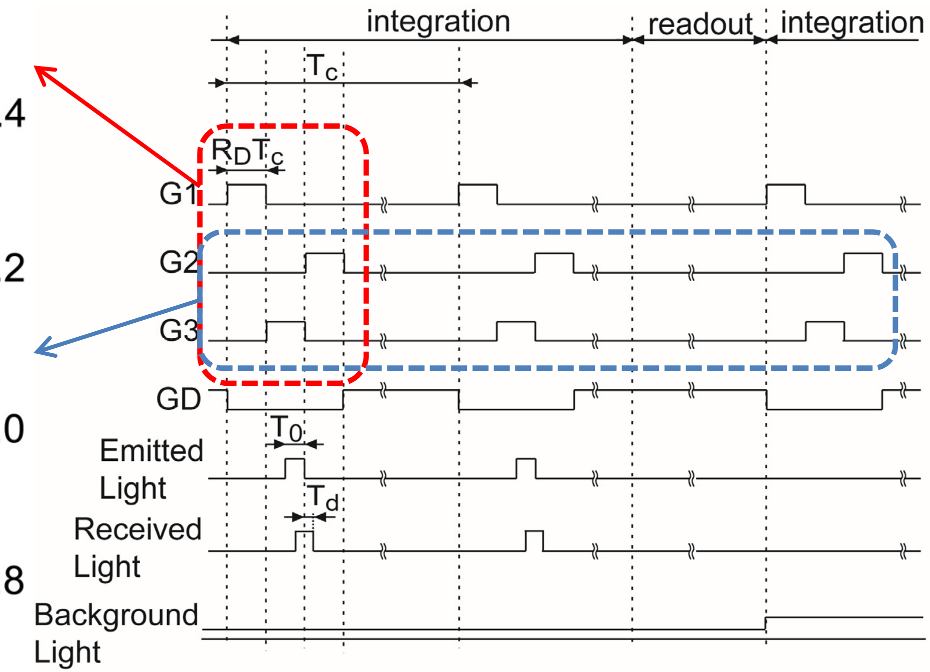


Standard deviation of 30 consecutive depth data averaged from the 100 pixels in the center of the array

Range images of a moving hand



Intensity Image



Performance comparison

Parameter	**This work**	Stoppa, et al.[4]	S. Kim, et al.[6]	W. Kim, et al.[7]
Resolution	**413 X 240**	64 X 64	500 X 274	480 X 270
Pixel Size (um^2)	**16.8 X 16.8**	30 X 30	14.6 X 14.6	2.25 X 9
Illumination Power (mW)	**250**	21 W/m^2 (peak power @ 1m)	700	450
Frame Rate (fps)	**15**	50/200	11 (Int. time 40ms)	-
Modulation Frequency(MHz), Light Pulse width(ns)	**13 ns (Light) 30 ns (Gate)**	25 MHz	20 MHz	20 MHz
Measured Range (m)	**0.8 ~ 1.8**	2~4.75 @ 50fps	0.75 ~ 4.5	1 ~ 7
Non-Linearity (%)	**1.03**	1.7	0.93	2.25
Range Resolution (mm)	**4.0 ~ 6.4**	19~57 @ 50fps	10 ~ 38 (with different int. time)	5~160
In pixel Background Cancelling	**Yes**	No	No	No
Frames to make Range image	**1 frame**	4 frame	2 frame	4 frame

Summary

- Sub-centimeter range resolution is obtained without background light
- Background light of moving objects is nicely cancelled by using in pixel background light cancelling technique.

A 0.3mm-Resolution Time-of-Flight CMOS Range Imager with Column-Gating Clock-Skew Calibration

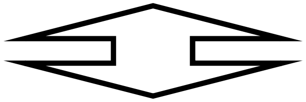
Keita Yasutomi, Takahiro Usui, Sangman Han
Taishi Takasawa, Keiichiro Kagawa,
Shoji Kawahito

Shizuoka University, Hamamatsu, Japan

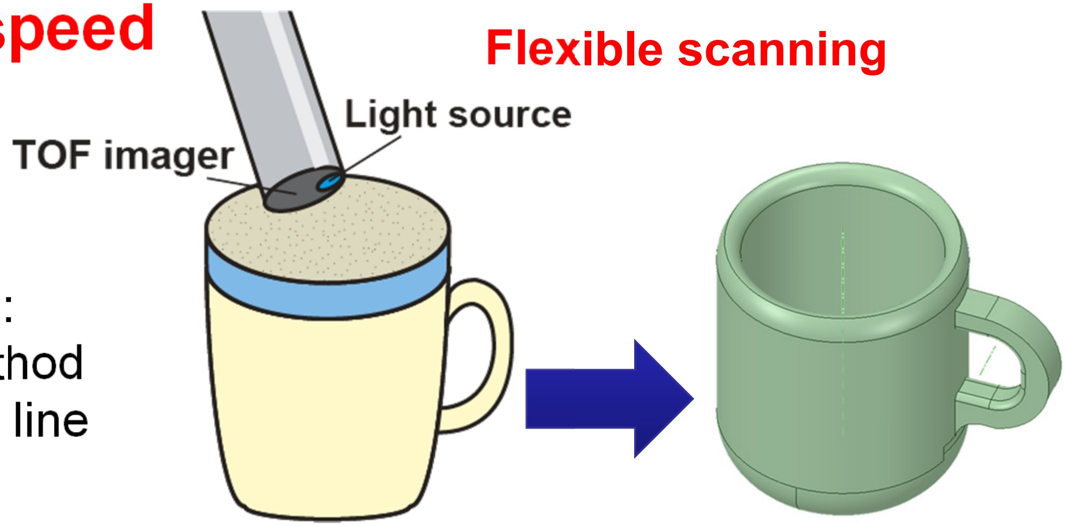
Motivation

New application for TOF range imagers

Miniature-head & **High-speed**
3D scanning system



Current contactless 3D scanners:
Light-section method
→ High resolution, but long base line



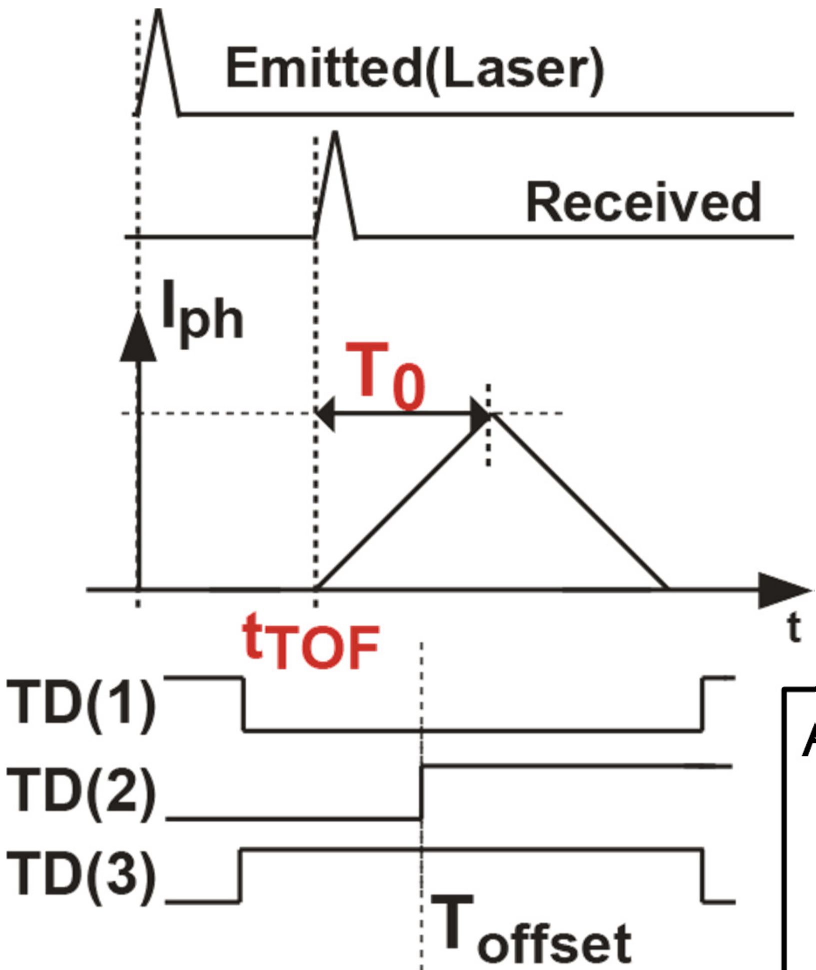
Challenges for sub-mm or higher range resolution

- Light source: short pulse width of <1ns
  → **Indirect TOF using impulsed light**
- High-speed modulation lock-in pixels
  → **Draining-Only Modulation (DOM) pixels**
- Column-wise skew of gating clocks
  → **Column-parallel skew calibration**

Proposed TOF Measurement Method

K.Yasutomi et al, IISW 2013

Concept: Use impulse response of photocurrent



$$t_{TOF} = T_{offset} - \mathbf{T_0} \cdot \sqrt{\frac{2(N_2 - N_3)}{N_1 - N_3}}$$

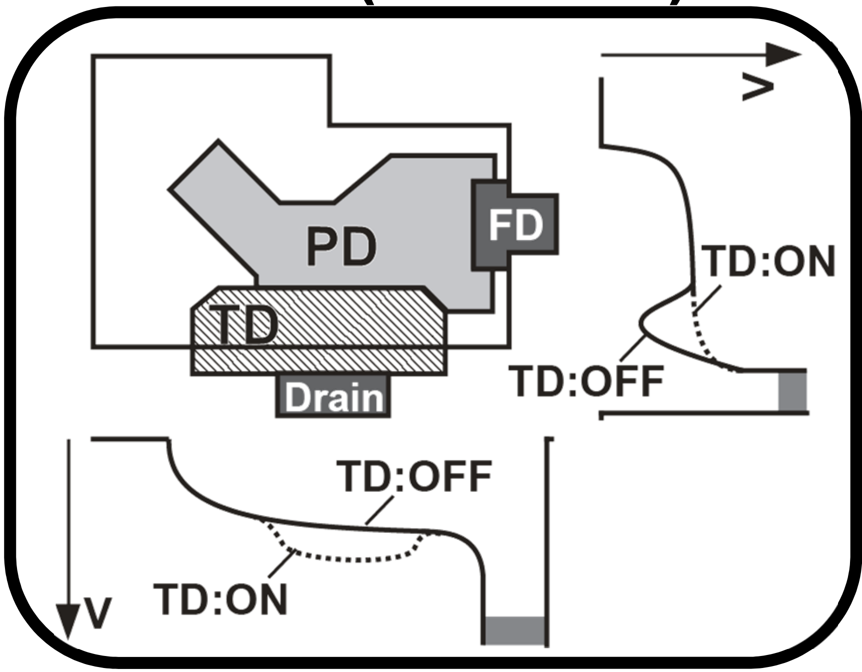
N_1,N_2,N_3: Signal electrons modulated by TD(1),TD(2),TD(3)

Advantages:
The photocurrent is regarded as an impulse response
→ Distortion of light pulse is negligible.

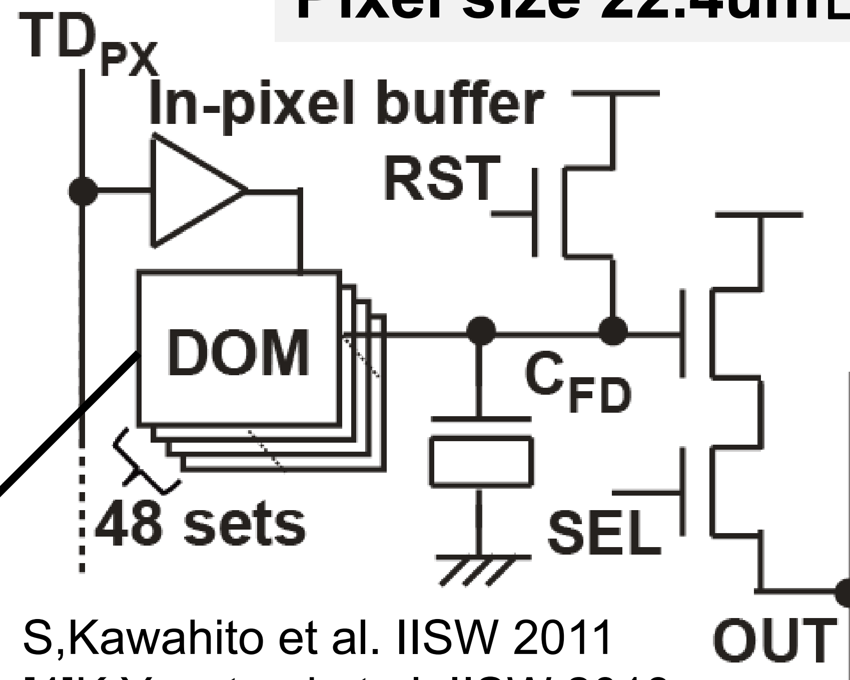
DOM Lock-in Pixel

DOM:Draining-Only Modulation

DOM unit (2.8um□)



Pixel size 22.4um□



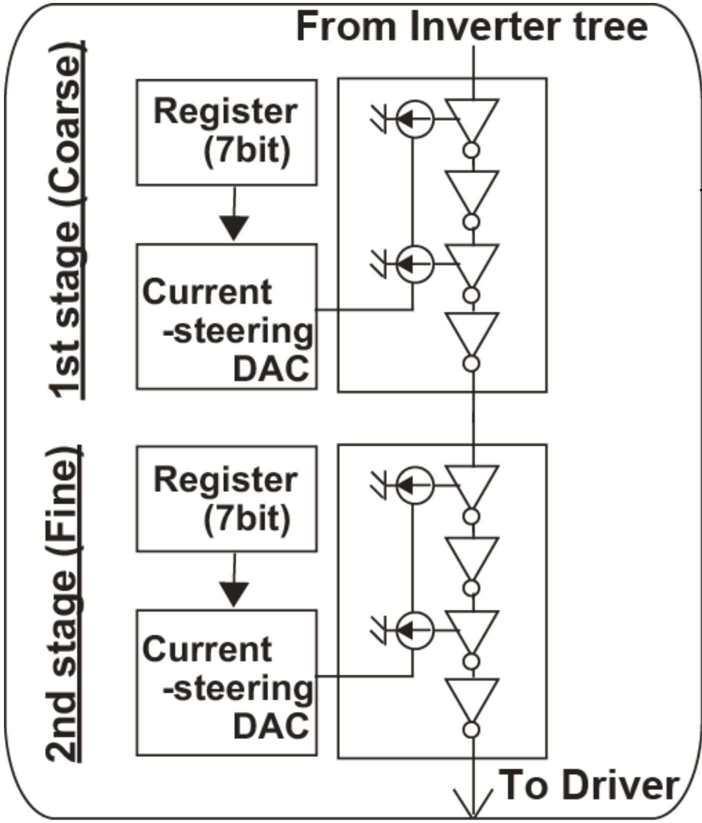
S,Kawahito et al. IISW 2011
[4]K.Yasutomi et al. IISW 2013
[5]Z. Li et al. TED 2012

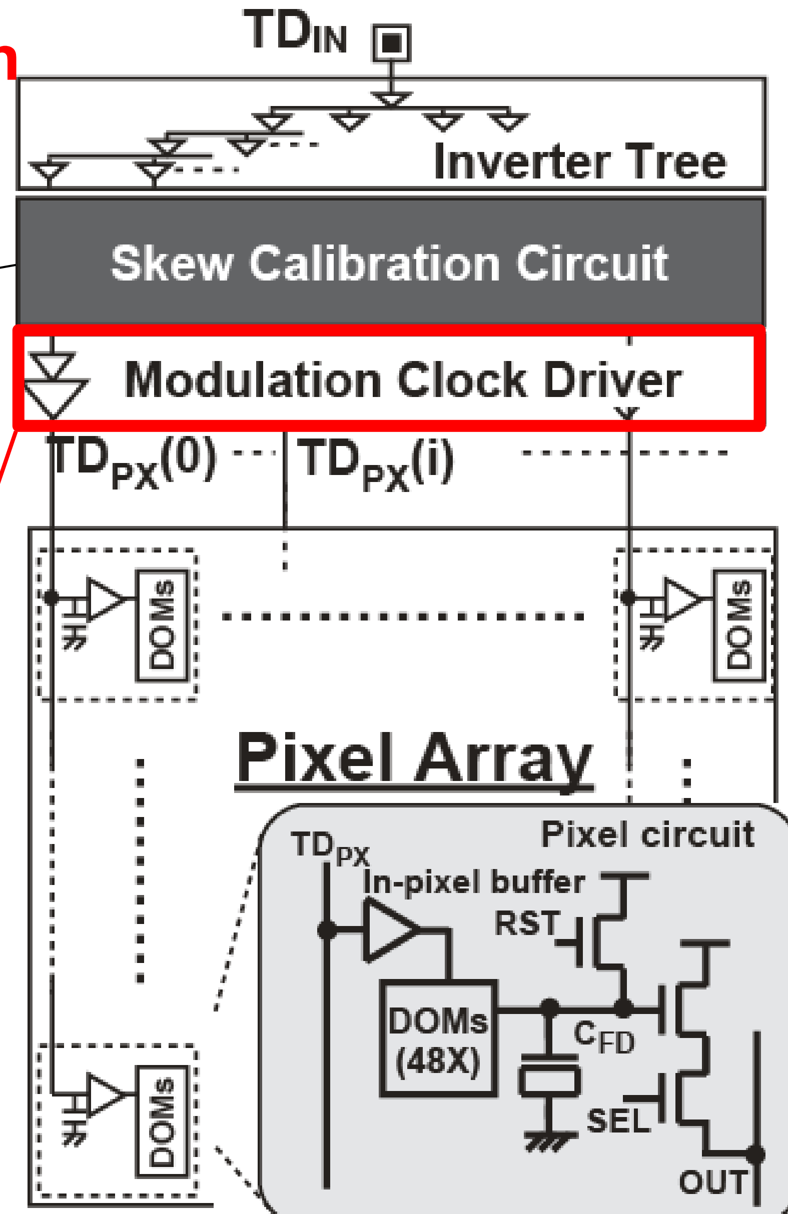
Advantages:

- DOM detector → **High-speed response**
  Loss-less repetitive accumulation
- In-pixel buffer → **Pulse shaping of TD**
  Reduced cap. of TD_{PX} wiring

Sensor Architecture

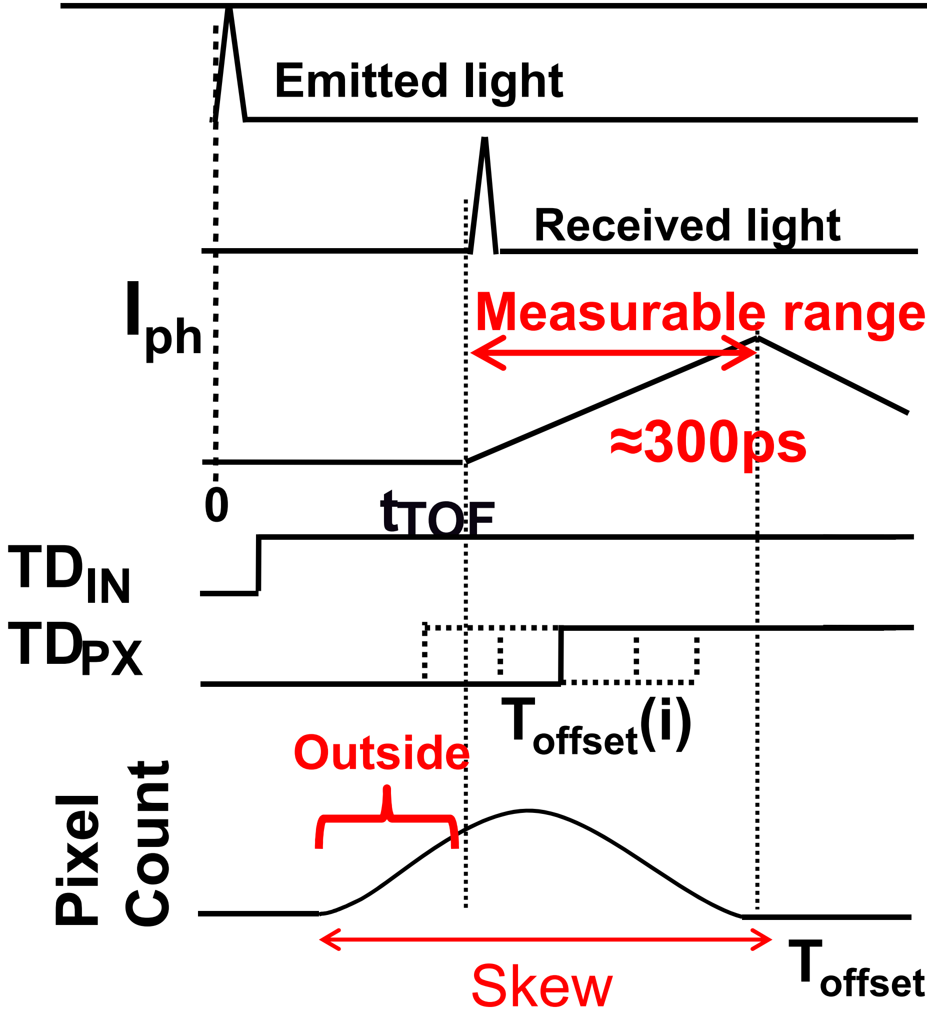
Column-parallel skew calibration

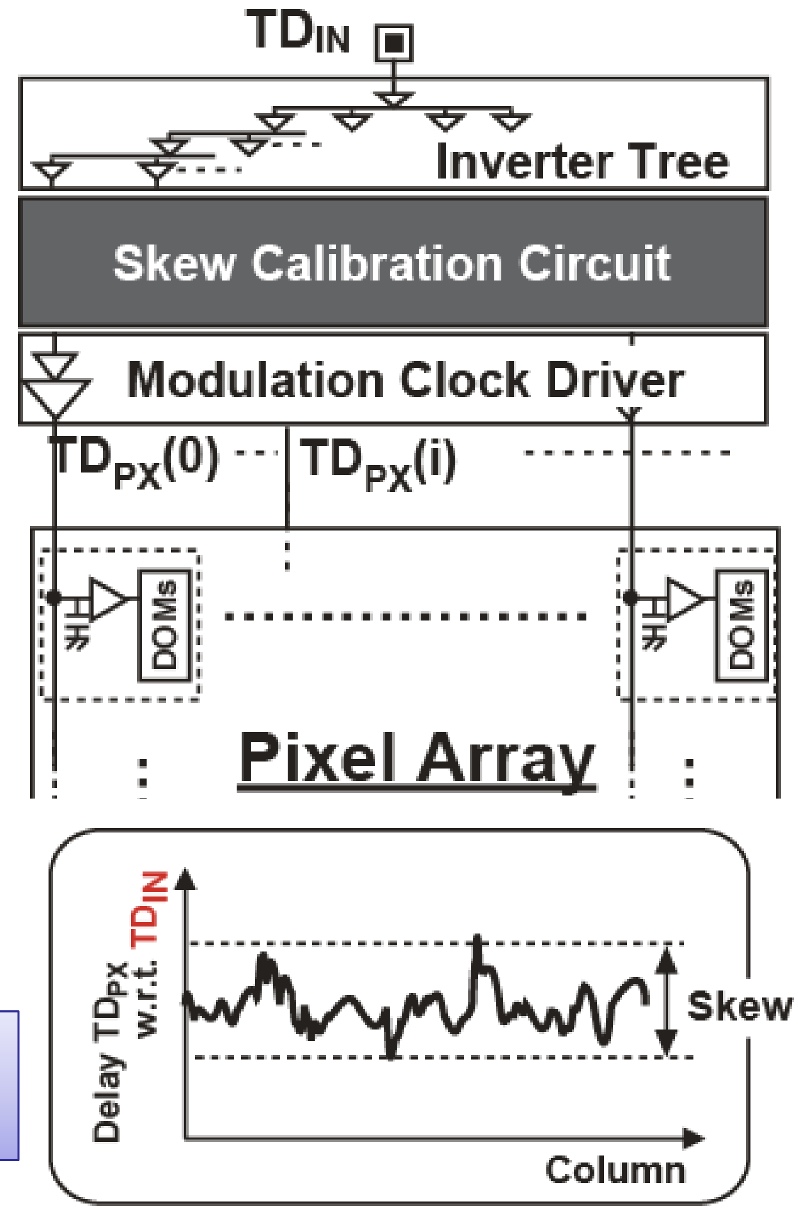




The skew between TD_{PX}s occurs due to device mismatch & voltage drop of the power supply line

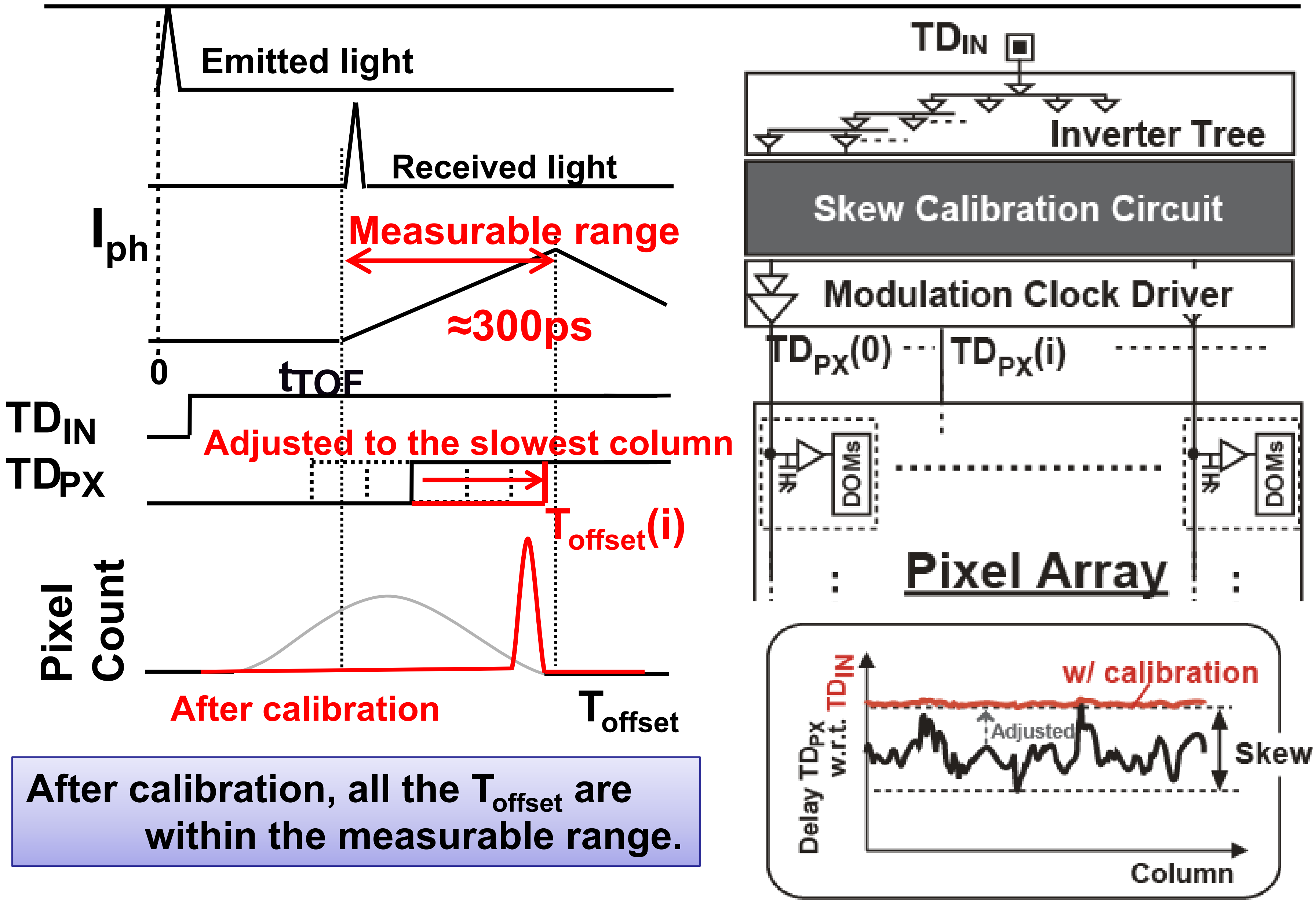
Why Skew Calibration Is Needed?





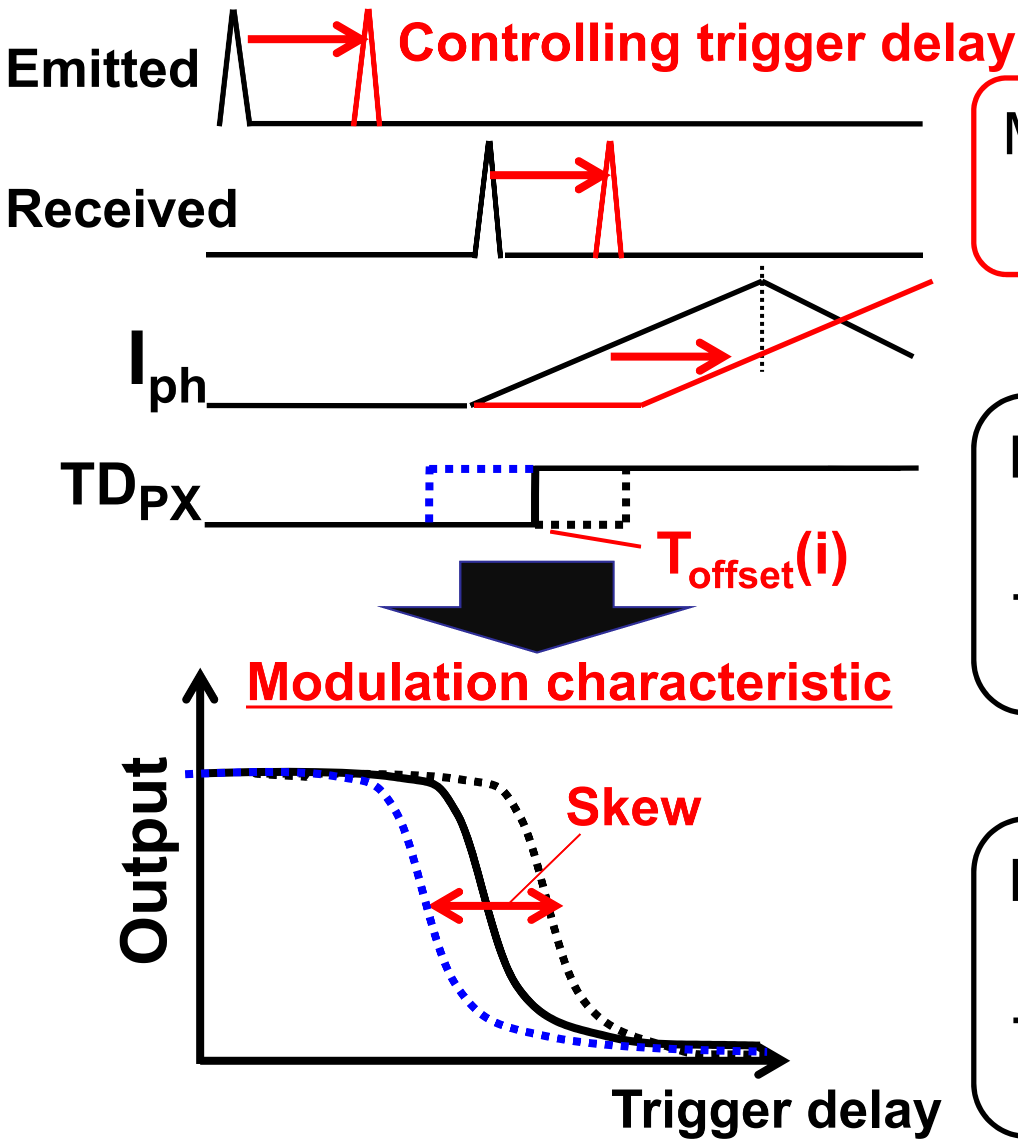
If the T_{offset} is outside of measurable range, the depth calculation is failed!!

Why Skew Calibration Is Needed?



After calibration, all the T_{offset} are within the measurable range.

Skew Calibration Procedure

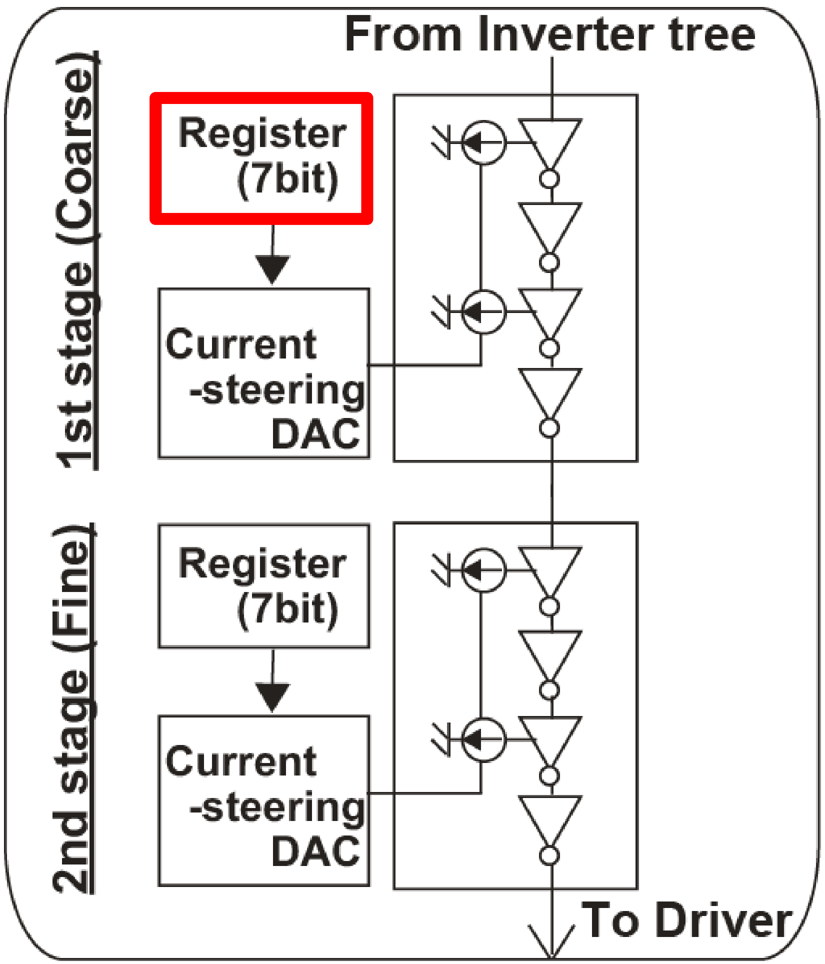


Measure the skew by controlling trigger delay.

Measure the delay while changing the 1st Reg. value.
→ The 1st Reg. value is chosen for minimized skew.

Measure the delay while changing the 2nd Reg. value.
→ The 2nd Reg. value is chosen for minimized skew.

Skew Calibration Procedure

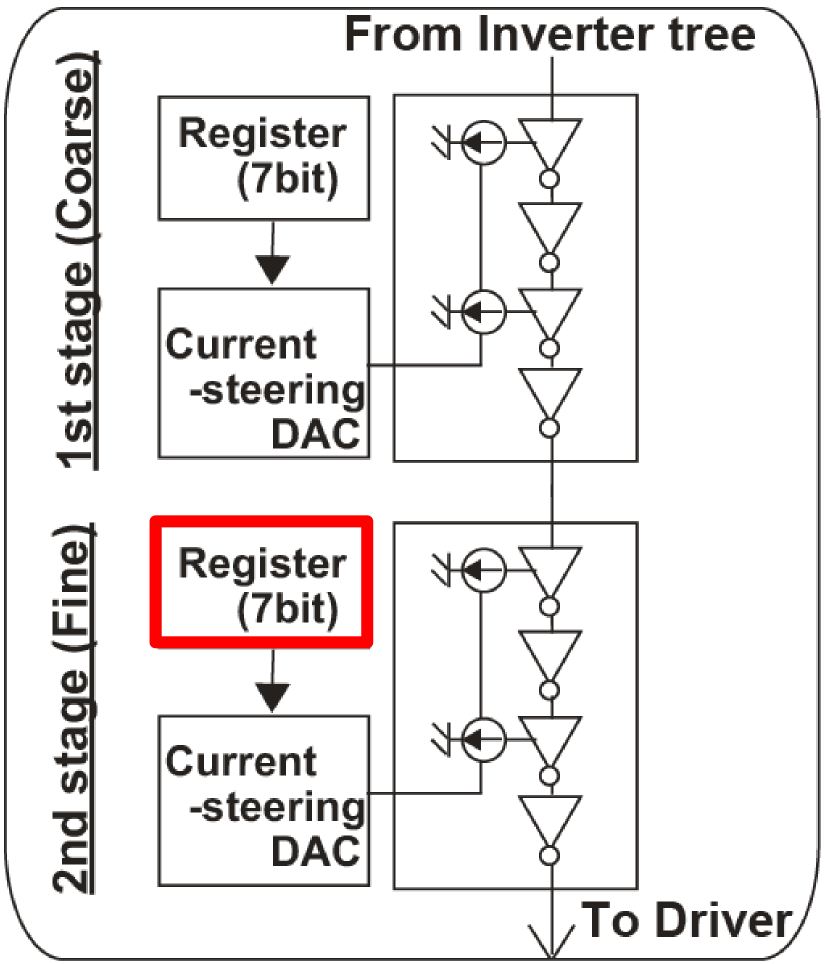


Measure the skew by controlling trigger delay.

Measure the delay while changing the 1^{st} Reg. value.
→ The 1^{st} Reg. value is chosen for minimized skew.

Measure the delay while changing the 2^{nd} Reg. value.
→ The 2^{nd} Reg. value is chosen for minimized skew.

Skew Calibration Procedure



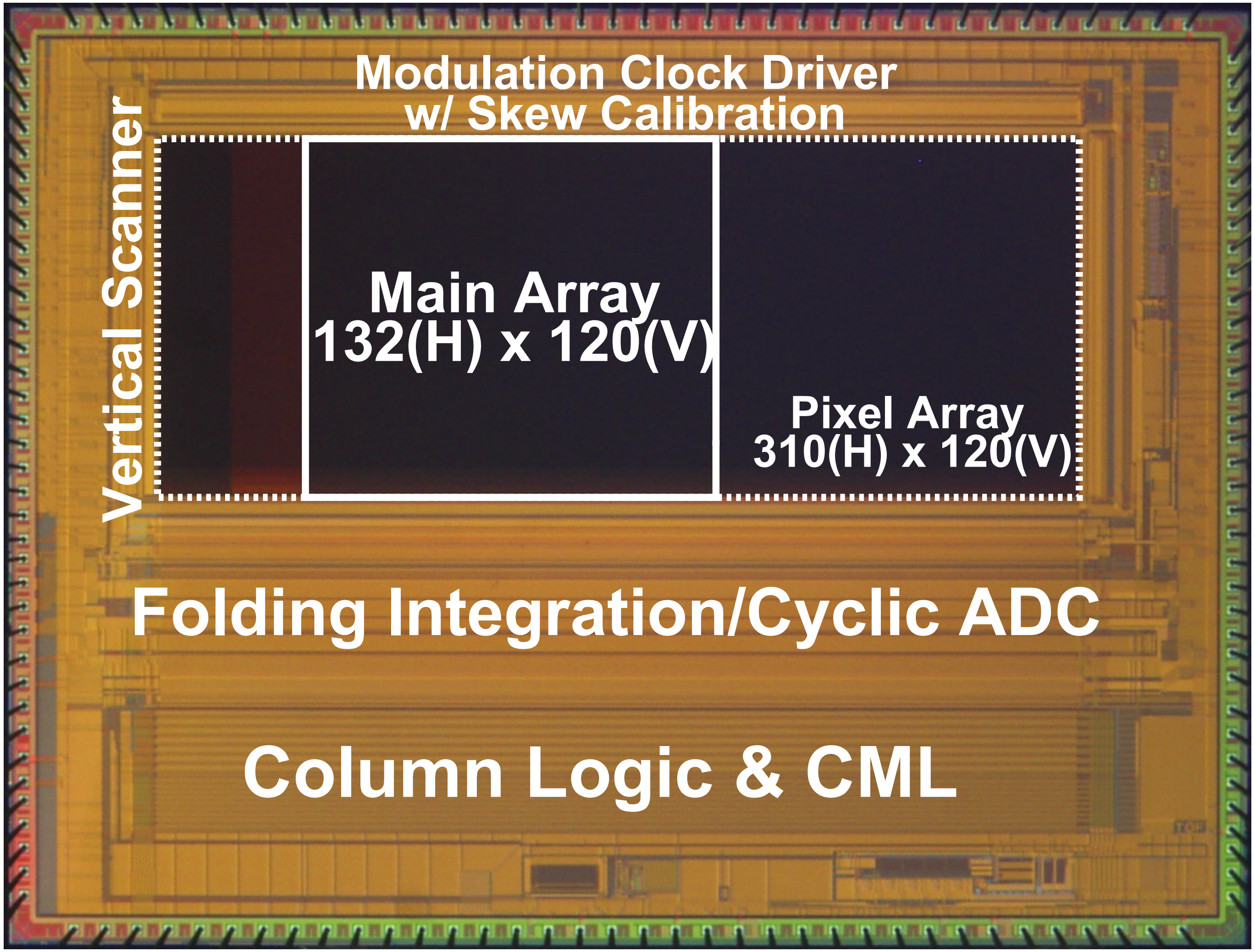
Measure the skew by controlling trigger delay.

Measure the delay while changing the 1st Reg. value.
→ The 1st Reg. value is chosen for minimized skew.

Measure the delay while changing the 2nd Reg. value.
→ The 2nd Reg. value is chosen for minimized skew.

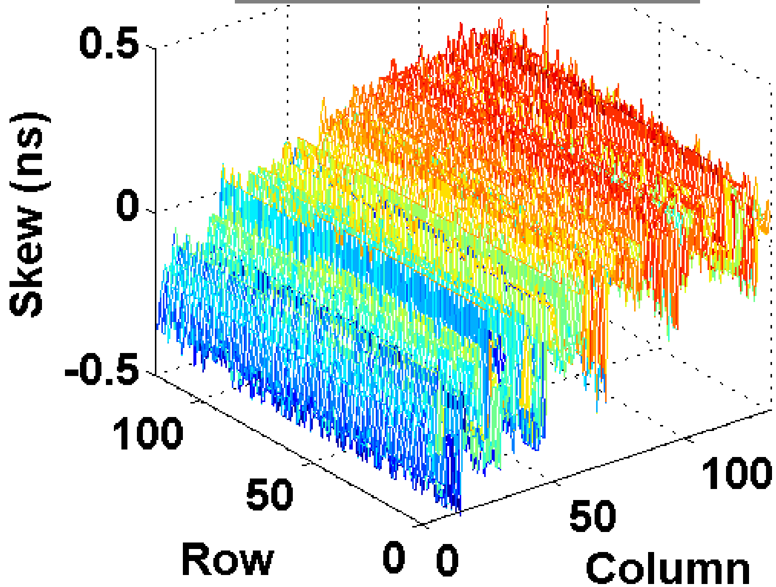
Chip Photograph

Technology: 0.11-um CIS
Pixel size: 22.4 x 22.4um^2

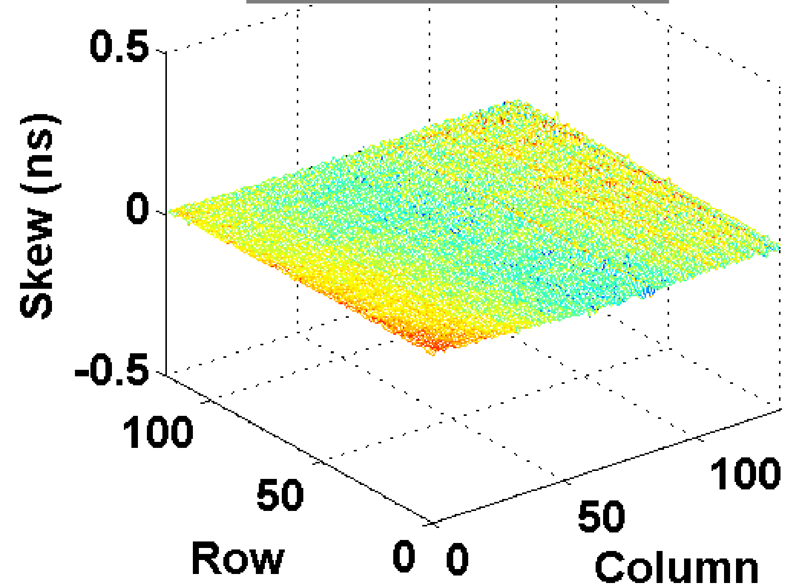


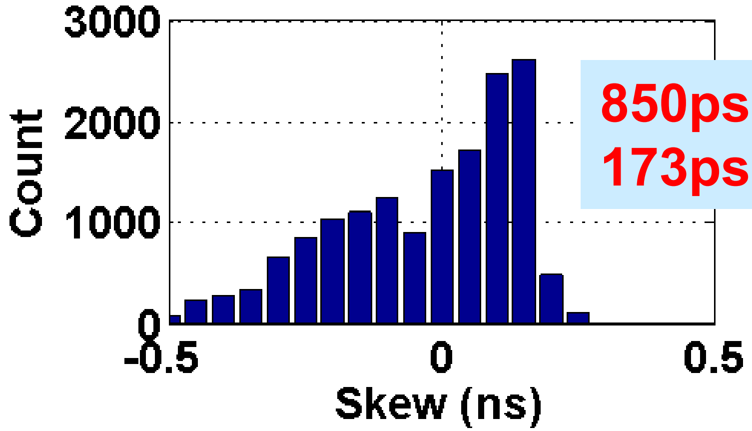
Measured Skew w/ Calibration

w/o Calibration

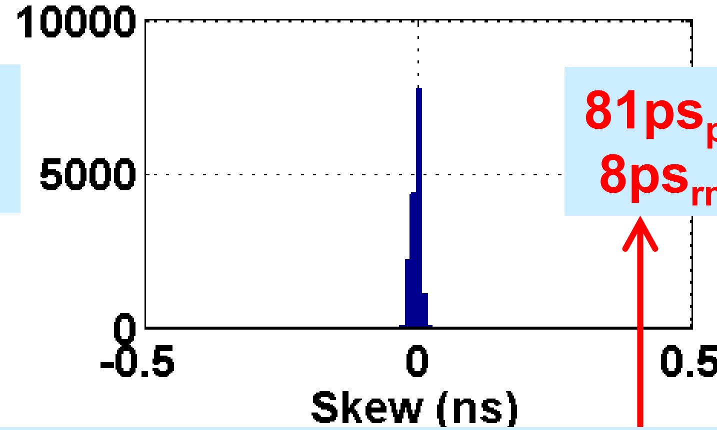


w/ Calibration





$850ps_{p\text{-}p}$
$173ps_{rms}$

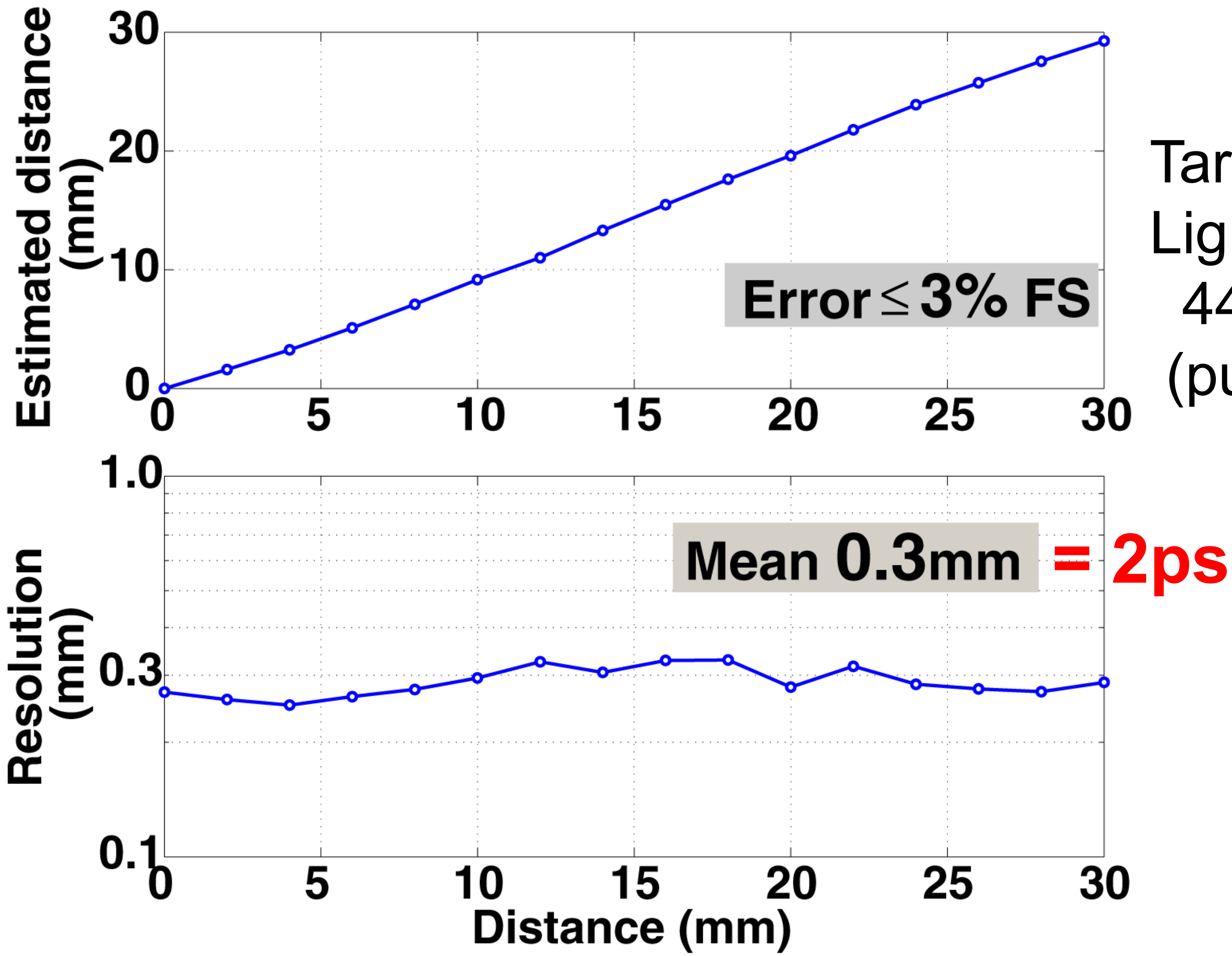


$81ps_{p\text{-}p}$
$8ps_{rms}$

Within the measurable range

Distance Measurement

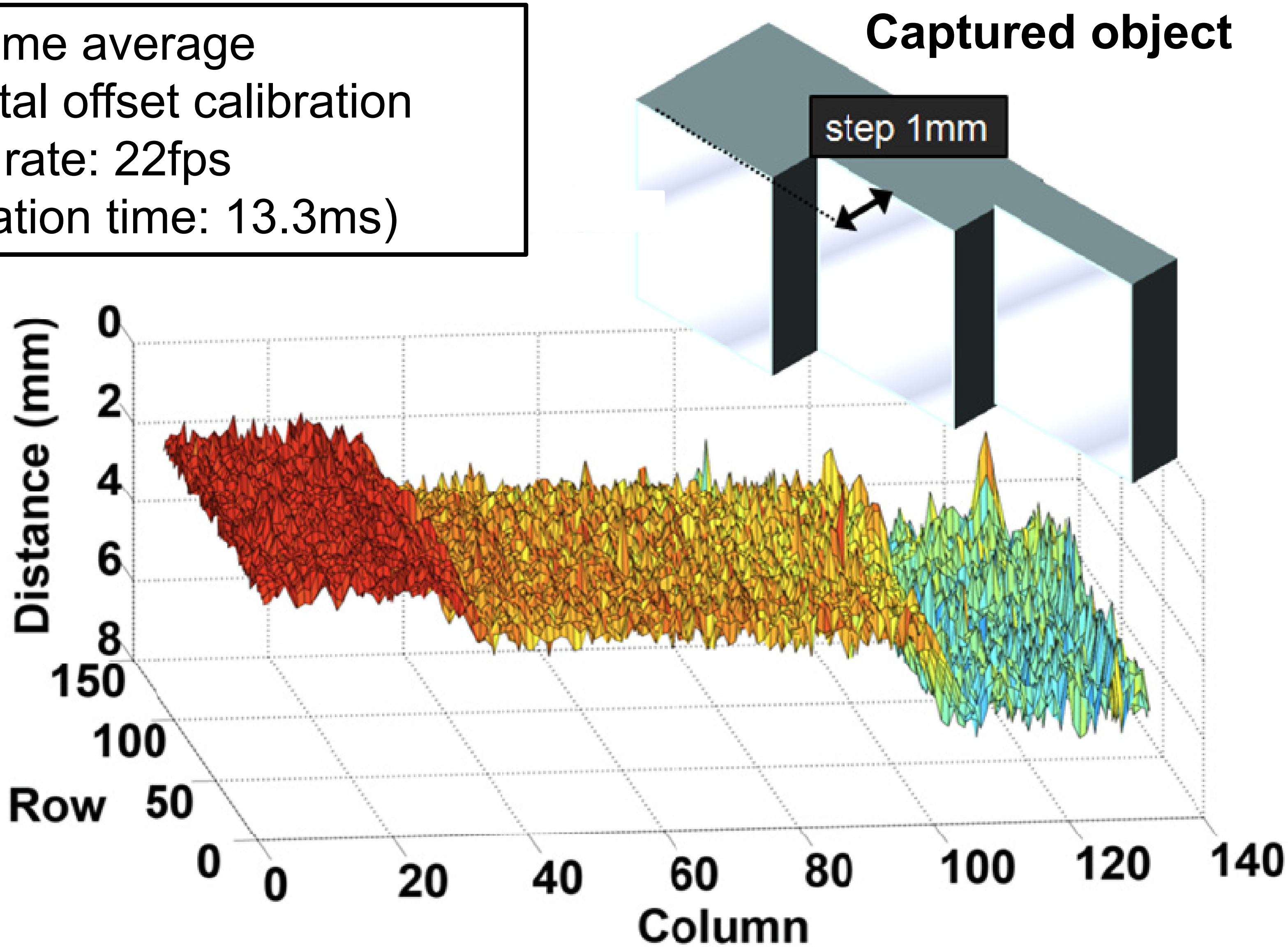
Average on all the main pixels.



Target: Mirror
Light source:
443nm laser
(pulse width 72ps)

Captured 3D image

- 500 frame average
- W/ digital offset calibration
- Frame rate: 22fps
  (Integration time: 13.3ms)



Performance Summary

Technology		0.11-μm CIS
Total pixels		310(H) × 120(V)
Effective pixels		132(H) × 120(V)
Pixel size		22.4 x 22.4 μm^2
Frame rate (Integration time 13.3ms/33ms)		22 fps / 9.6 fps
Repetition frequency		7.5 MHz
Fill factor (without micro-lens)		24 %
Emitter	Wavelength	443 nm
	Pulse width	71.6 ps
	Power	12.5 $\mu W/cm^2$ at focal plane
Measurable range		32 mm at error < 3% Full scale
Range resolution		0.3 mm (mean in measurable range)

Performance Comparison

Spec.	[1]	[2]	[3]	[4]	[5]	[6]	This work
Technology [um]	0.18	0.11	0.35	0.13	0.35	0.35	0.11
Pixel no.	80x 60	320x240	336x252	480x360	64x64	60x48	132x120
Pixel pitch [um^2]	10	12	15	10	30	85	22.4
Fill factor [%]	24	34.5	19	24	25.75	0.5	22
Wavelength [nm]	850	850	870	850	850	850	443
Accumulation time	50ms	50ms	330ms (3fps)	10ms	20ms (50fps)	45ms	33ms
Range resolution @Measured distance	50mm @1m	10mm @1m	7.4mm	5mm @1m	19mm @2m	5mm @40cm	**0.3mm** @32mm

[1] D.Stoppa, et al., JSSC, 2011.
[2] S-J. Kim, et. al. JSSC, 2012.
[3] S.Kawahito, et.al. " Sensors J., 2007.
[4] W.Kim, et.al. ISSCC 2012.
[5] Shcherbakova, et.al, ISSCC 2013
[6] C.Niclass, et.al,JSSC, 2009..

Summary

- Indirect TOF technique using implused light
- DOM lock-in pixels provide:
  - **high-speed charge modulation**
  - Loss-less repetitive accumulation
- **Column-parallel skew calibration** achieves:
  skew is reduced from $850ps_{p\text{-}p}$ to $81ps_{p\text{-}p}$
- Prototype sensor demonstrates:
  0.3mm resolution @ 32mm range.
  (= **2ps** time resolution)

XBOX ONE

7.6 - A 512×424 CMOS 3D Time-of-Flight Image Sensor with Multi-Frequency Photo-Demodulation up to 130MHz and 2GS/s ADC

A. Payne, A. Daniel, A. Mehta, B. Thompson, C. S. Bamji, D. Snow, H. Oshima, L. Prather, M. Fenton, L. Kordus, P. O’Connor, R. McCauley, S. Nayak, S. Acharya, S. Mehta, T. Elkhatib, T. Meyer, T. O’Dwyer, T. Perry, V-H. Chan, V. Wong, V. Mogallapu, W. Qian, Z. Xu

February, 10th 2014

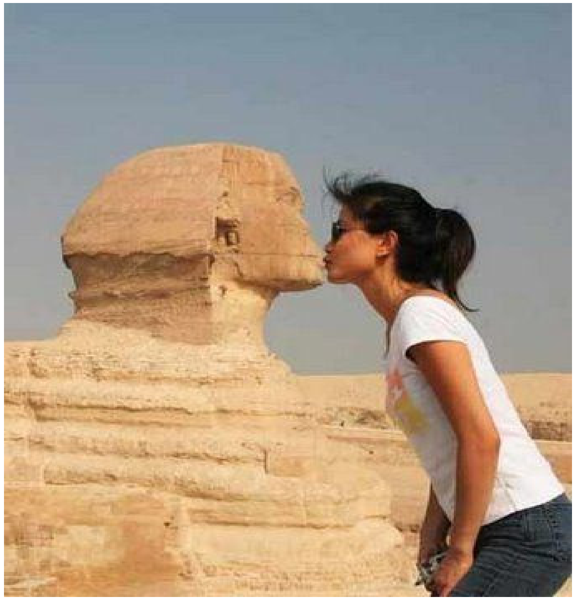
Microsoft

Outline

- Introduction
- Theory of Time-Of-Flight (TOF)
- Chip components
  - Pixel
  - Column Amplifiers and ADC
  - Digital
- Measured results
- Summary

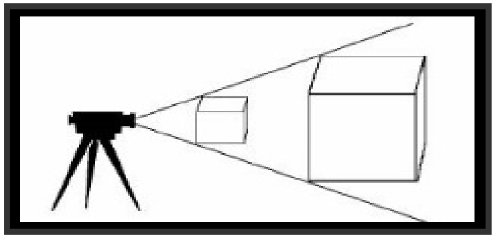
Why 3D (Depth) Imaging?

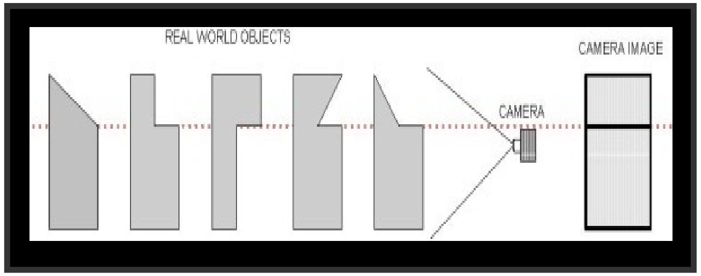
1. 2D Image analysis is tricky



voillusions.blogspot.com

2. Objects of different sizes and shapes can appear the same

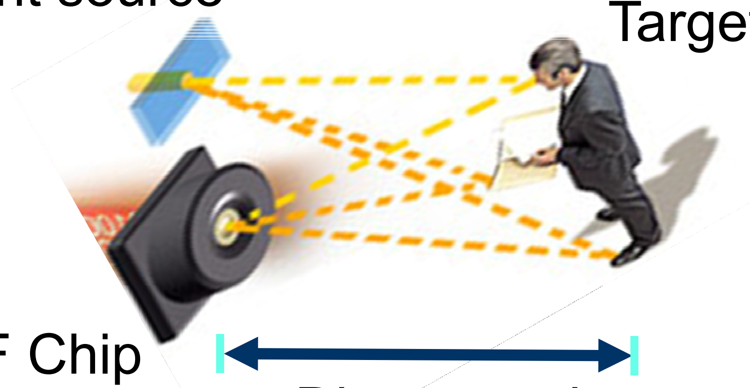




3D System Requirements for Games

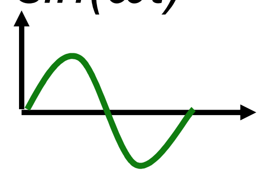
- Large play space
  - 70^o x 60^o FOV
  - 0.8m~4.2m distance range
- Detect small objects at a distance
- 68dB brightness system dynamic range (must meet spec in range)
  - Variation from target distance (0.8m-4.2m)
  - Variation from target reflectivity (15%~95% with ambient)
- Indoor ambient lighting
- Motion blur resistant

Theory of Operation (Phase Detection)



$sin(\omega t)$

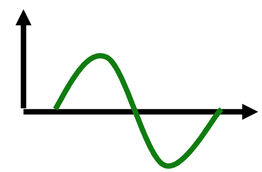
Transmitted Signal



Active IR

$A sin(\omega t - \Phi) = A sin(\omega(t - 2d/c))$

Reflected Signal

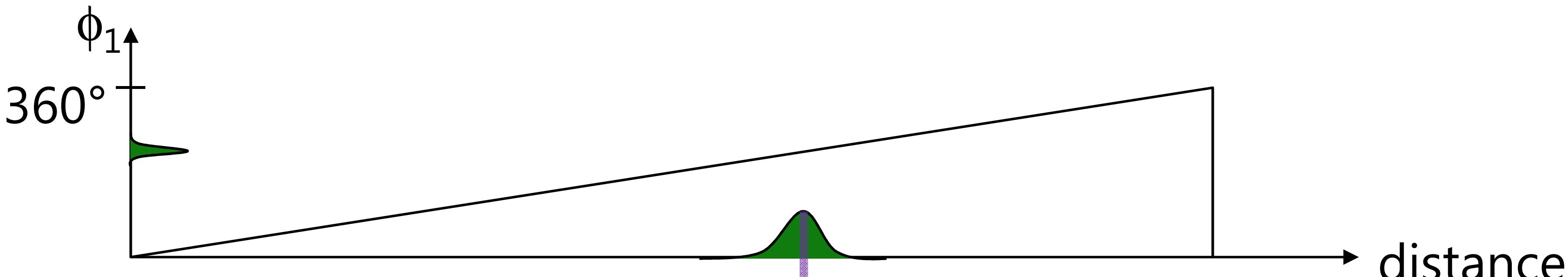


$\Phi = 2d\omega/c$

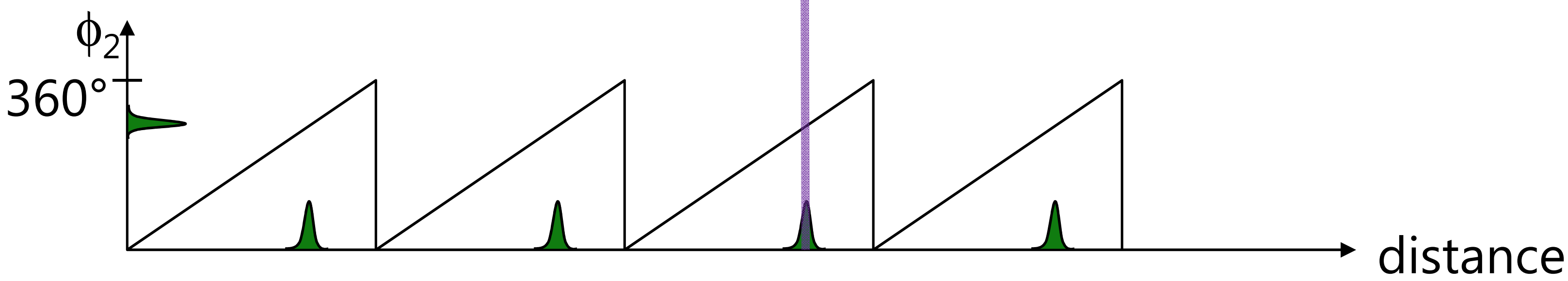
detected phase= depth

Modulation Frequency Tradeoffs ($d = \Phi c/2\omega$)

- Low frequency has *no* ambiguity but large depth uncertainty

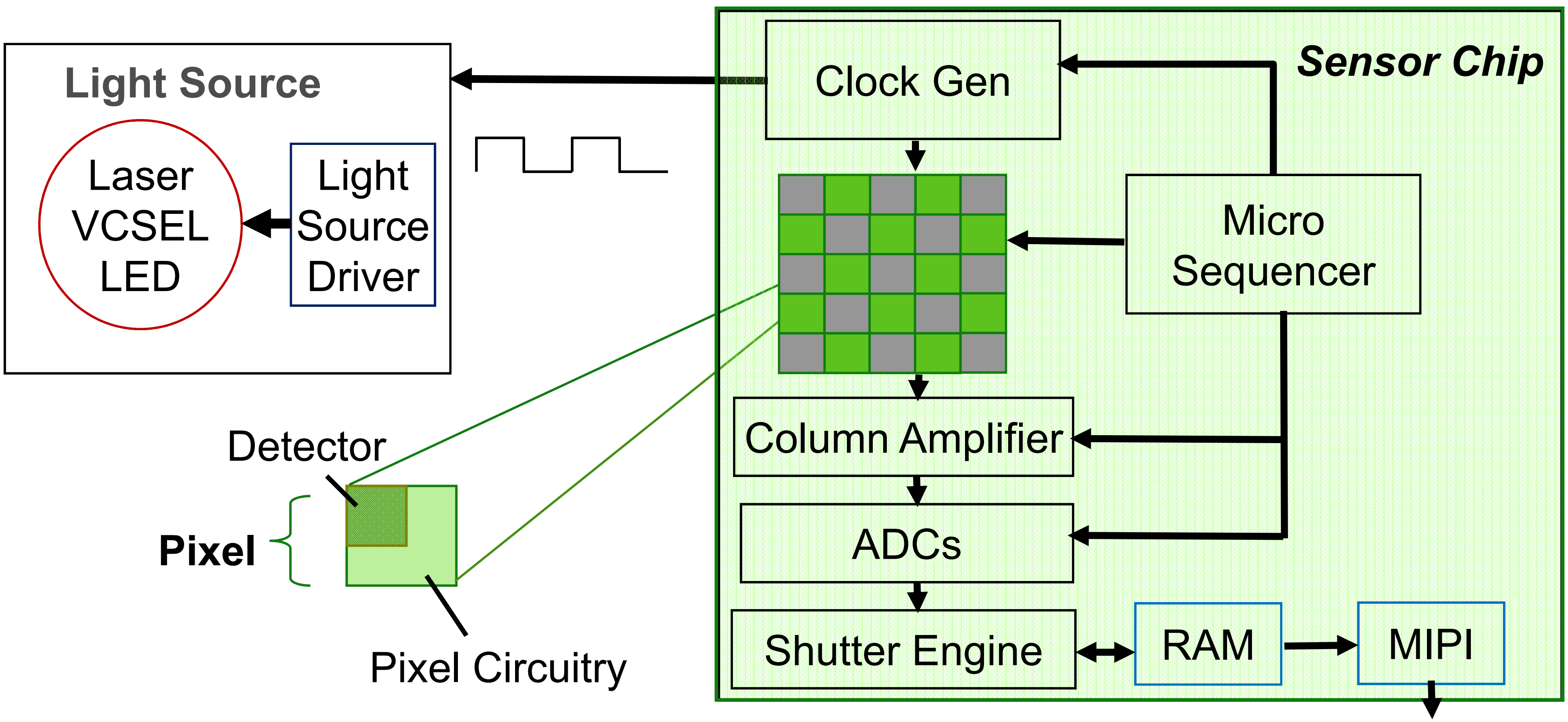


- High frequency has more ambiguity but small depth uncertainty

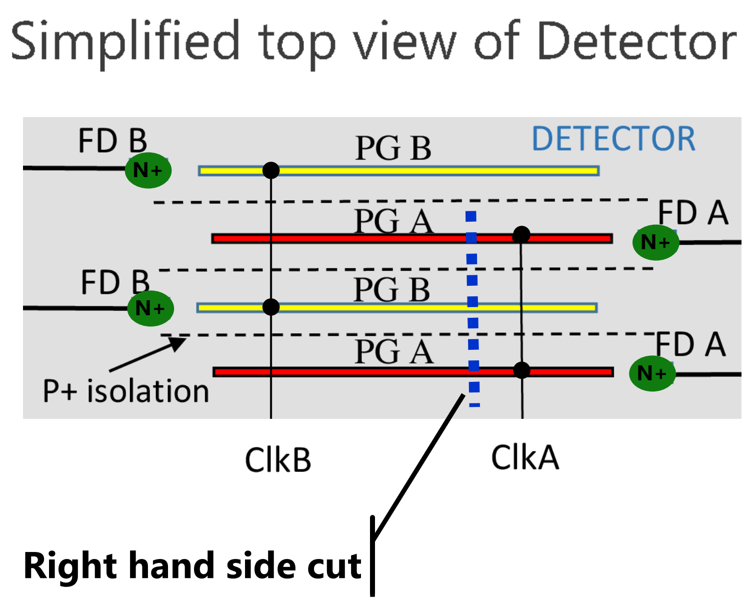


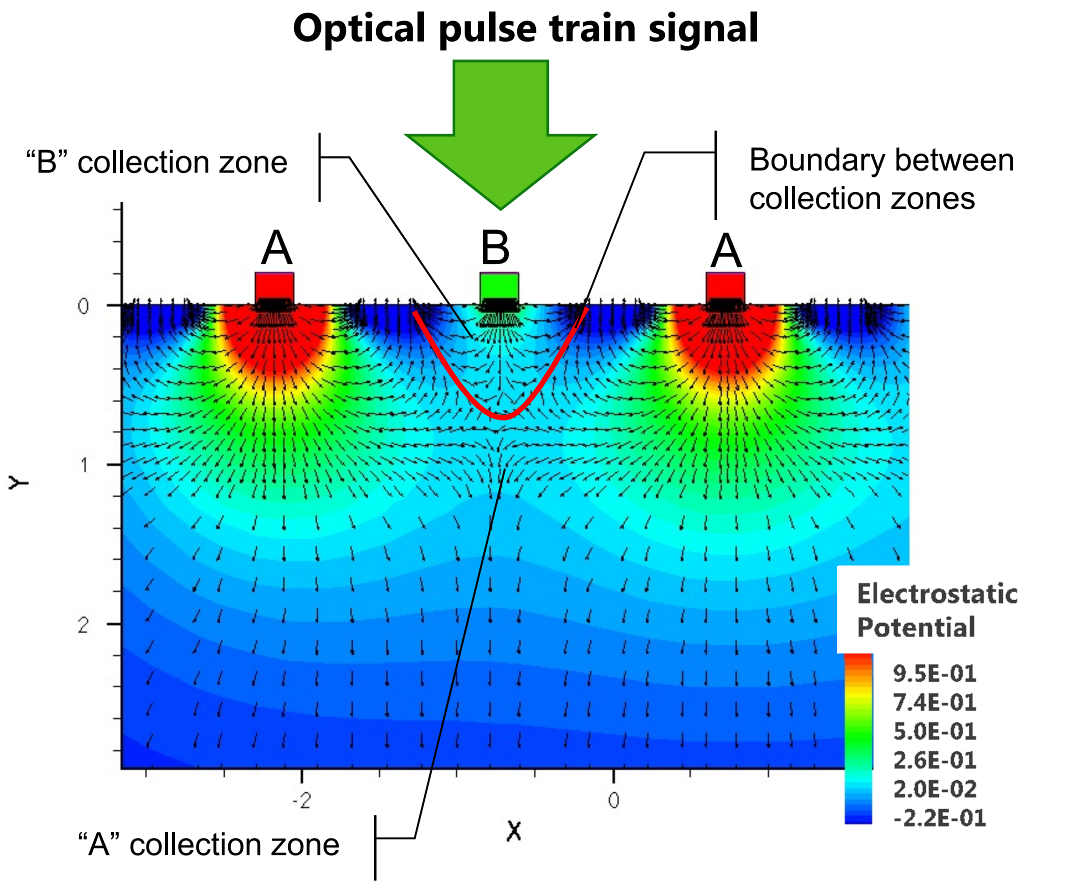
- Multi-frequency: Best of both worlds

System Architecture



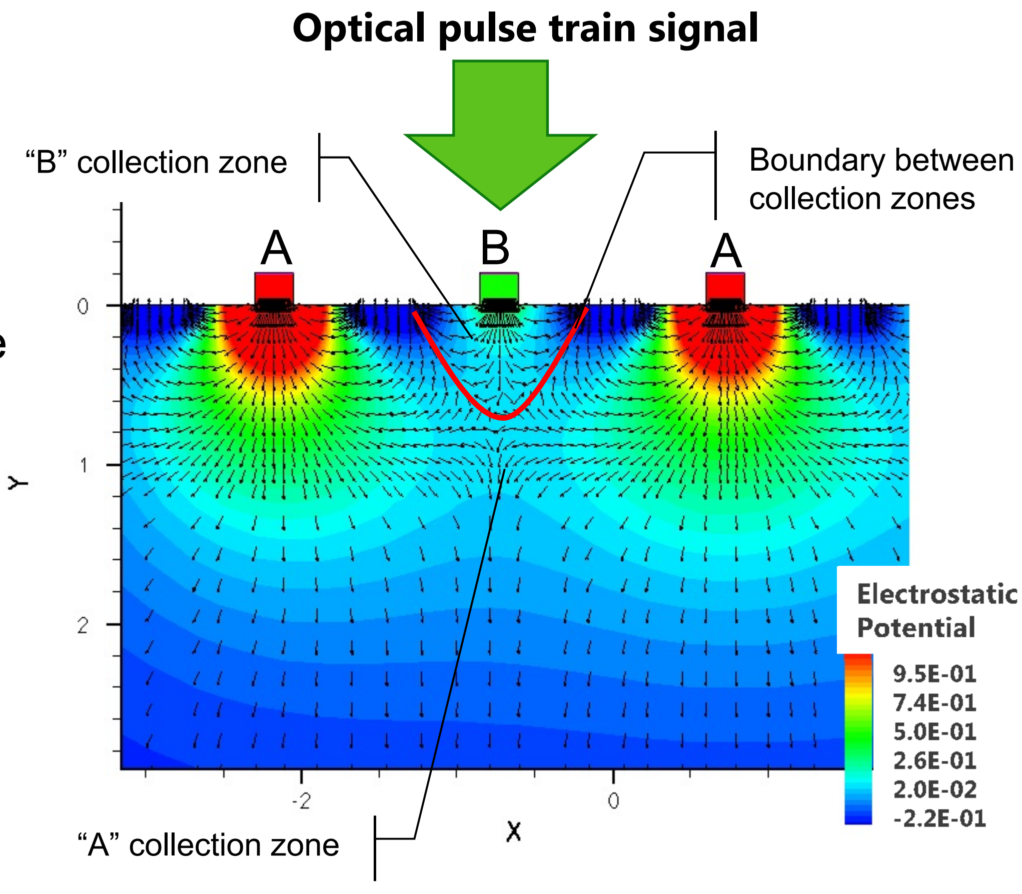
Pixel Design (Differential TOF Phase Detector)



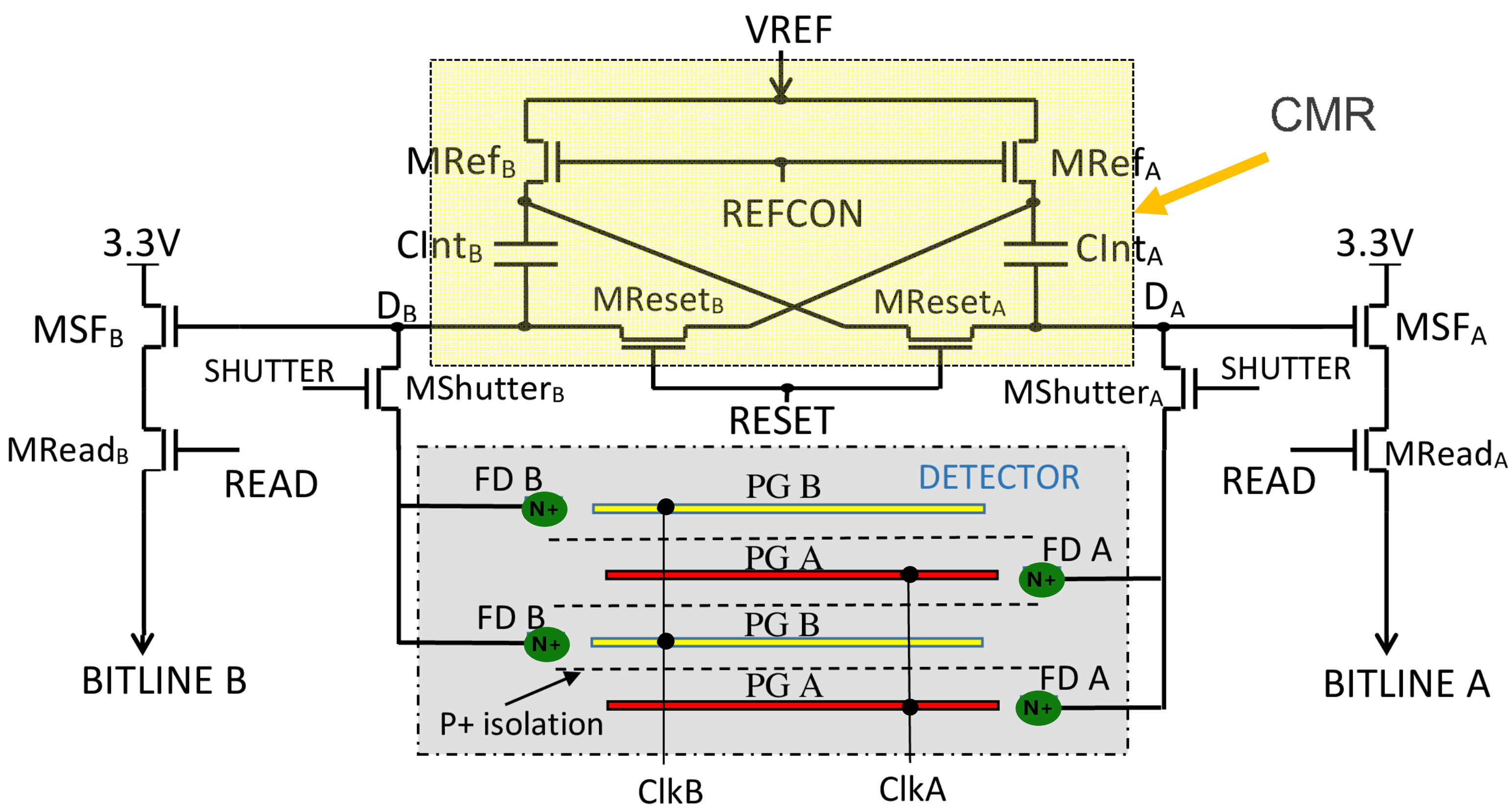


Pixel Design (Differential TOF Phase Detector)

- A and B alternate high/low
- Light synchronized with A/B clock
- When A is high most electrons are captured by A
- When B is high most electrons are captured by B
- Arrival time of light can be estimated by (A-B)/(A+B)



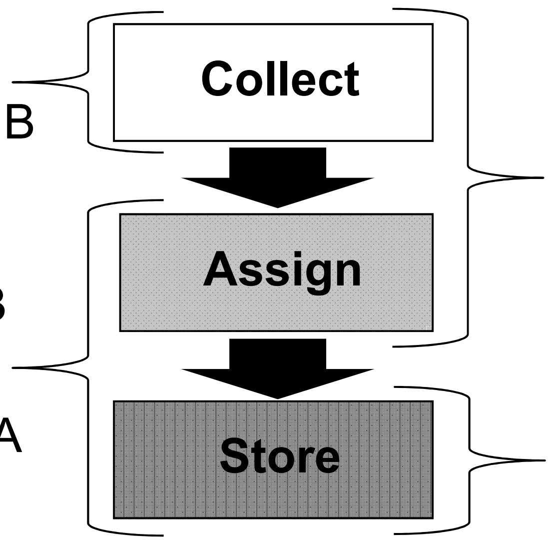
TOF Pixel Design (Differential Pixel Schematic)



Time of Flight Detection

Charge Transfer (CCD-like)

- Charge collected before being assigned to gate A or B
- Charge transferred to A or B
    - Charge stored in n+ to complete assignment to A or B

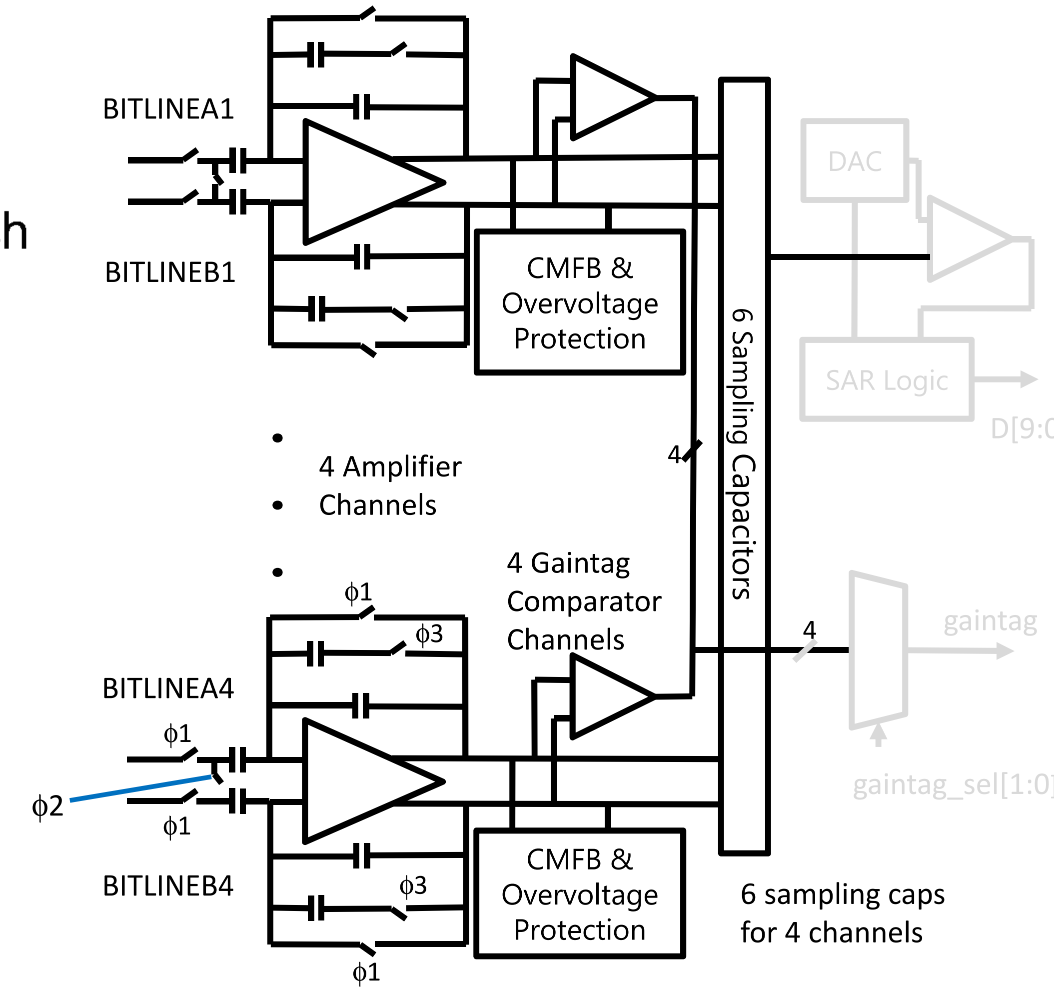


Quantum Efficiency Modulation (This Work)

- Charges collected and simultaneously assigned to gate A or B
- n+ storage advantageously decoupled from charge assignment
    - Charge collection at n+ can happen *at leisure*

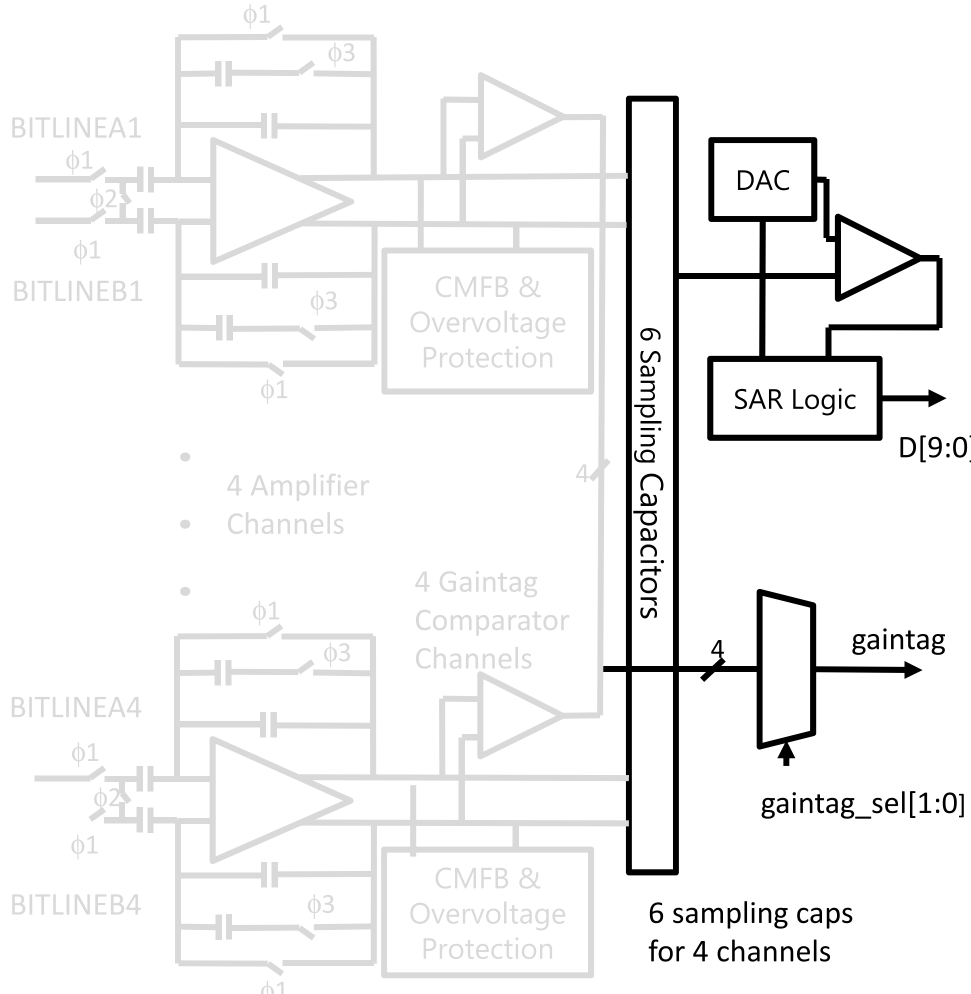
Column Amplifiers

- 2x512 amplifiers on 10μm pitch
  - Switched capacitor
  - Offset cancelled
  - Variable dual gain (1x~16x)
  - Overflow detection
  - 1% gain matching
  - 3.3V rail to rail input CM
  - Output at 1.5V



ADC

- 2x128 ADC on 40μm pitch
  - 10-bit charge-redistribution SAR
  - 8-bit ENOB
  - 8MS/s (10 cycles at 80MHz)
  - 0.027mm^2
  - 1.5V operation
- Total conversion capacity >2GS/s
- Full frame conversion in <110μs

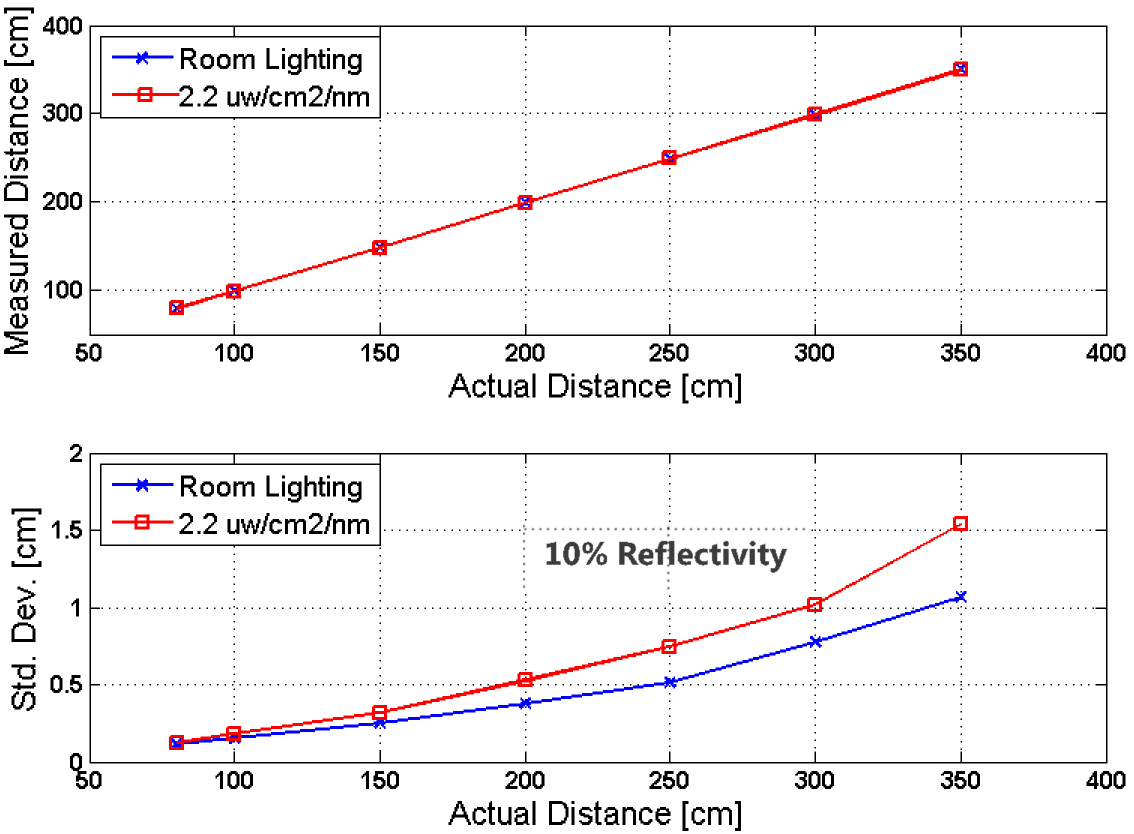


Micro-Sequencer, Shutter Engine & Serial I/O

- Micro-Sequencer
  - Executes micro-instructions controlling the sensor (e.g. shutter, frequency)
    - Any choice of multi-phase, multi-shutter, multi-gain, multi-frequency
      - Example sequence : [set frequency to 100Mhz],[reset array],[integrate with shutters 0.5ms, 2ms] [ADC] etc..
- Shutter Engine
  - CDS (differential) and multi-shutter/gain selection for extended dynamic range
  - Integrated frame buffer reduces the I/O bandwidth required by the chip
- High-Speed Serial I/O
  - Two 4-lane MIPI D-PHYs
  - 8Gb/s I/O bandwidth

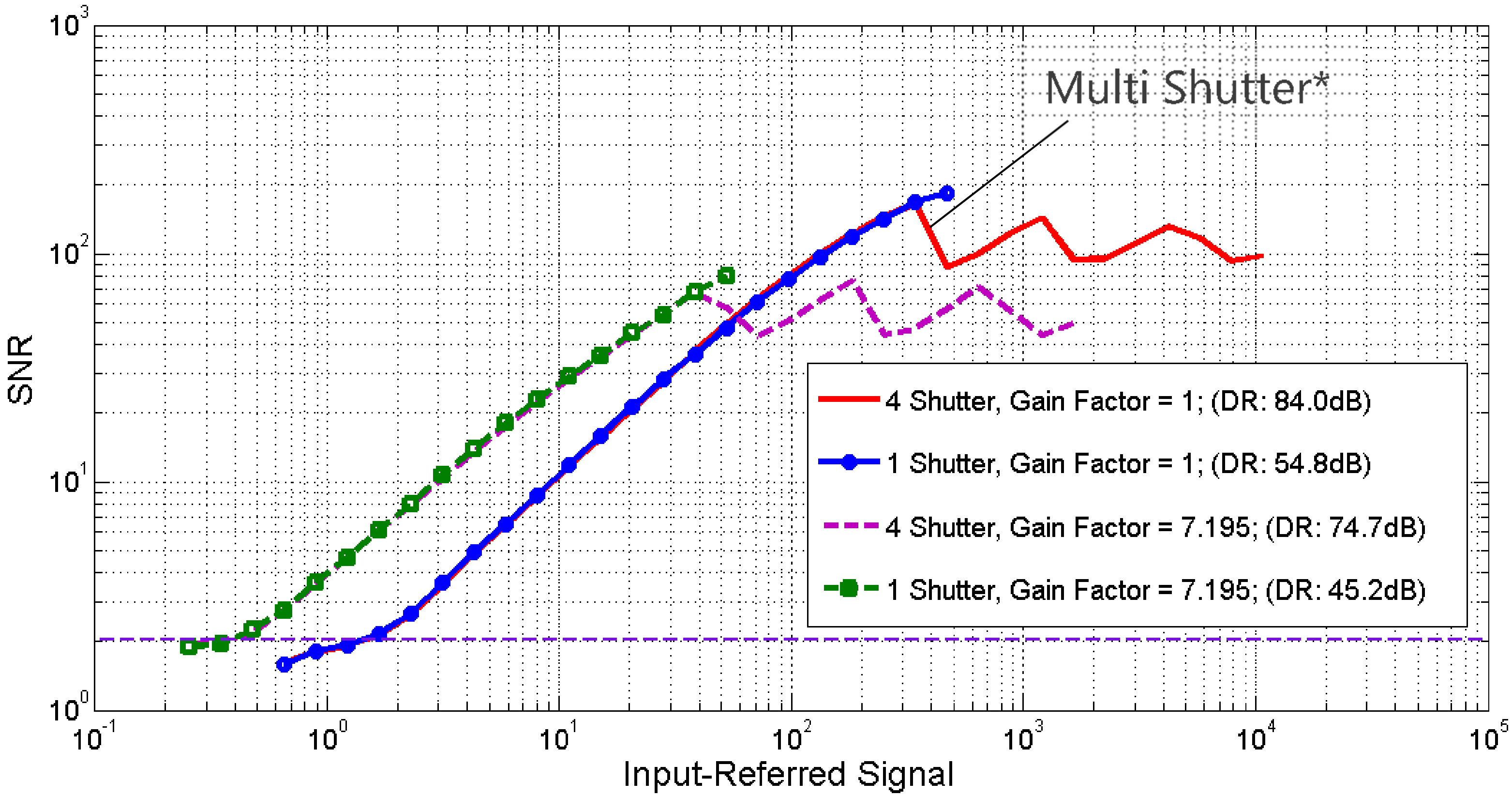
Measured Depth Accuracy

- Depth Range
  0.8m~3.5m (4.2m radial)
- Accuracy Error
  Better than 1%
- Depth uncertainty
  <0.5% of actual distance



Multi-Shutter & Multi-Frequency

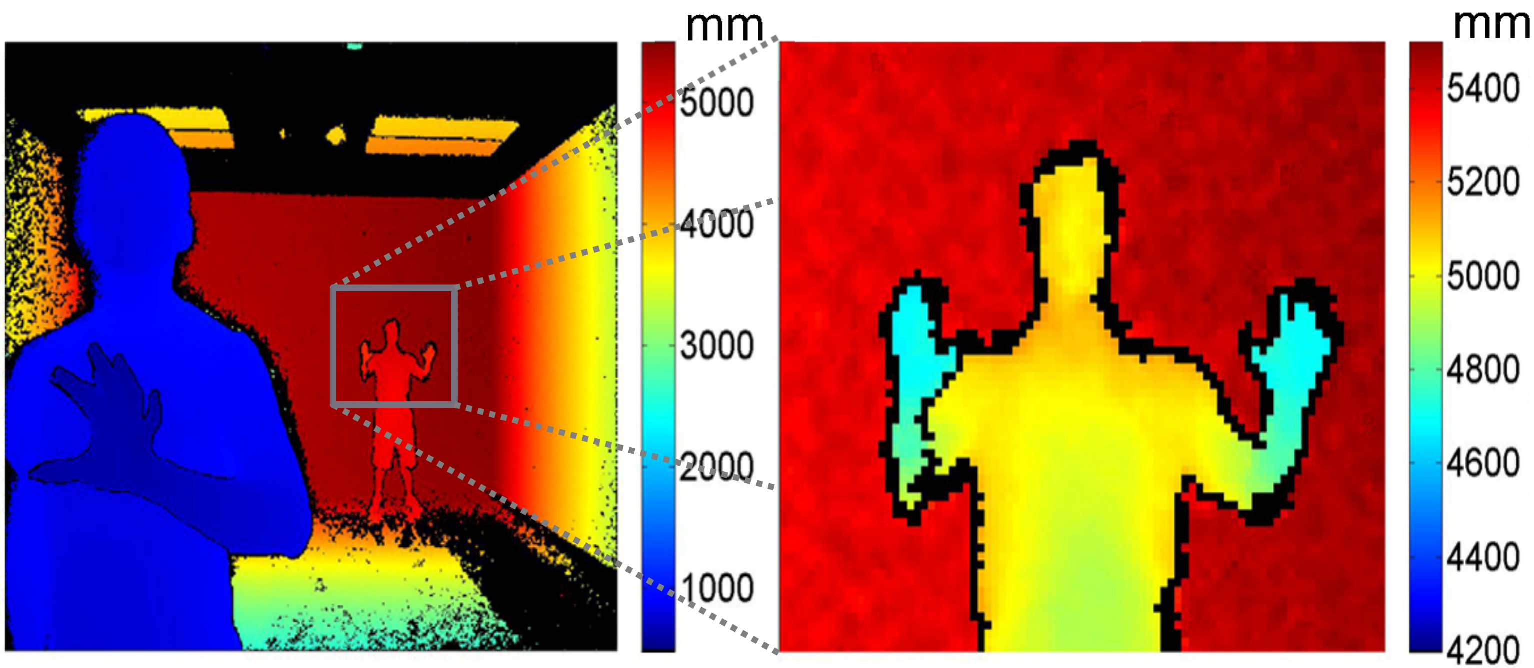
Measured Dynamic Range



* Each Pixel selects its own best shutter for high dynamic range

Measured Depth Range

- Room lighting
- 30fps
- 3x3 spatial filter

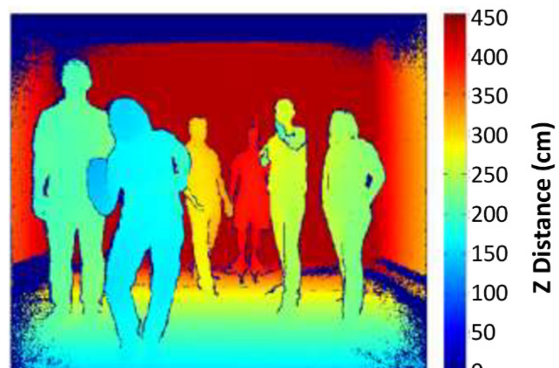


Shows 1-5m operation with no aliasing

Depth Images

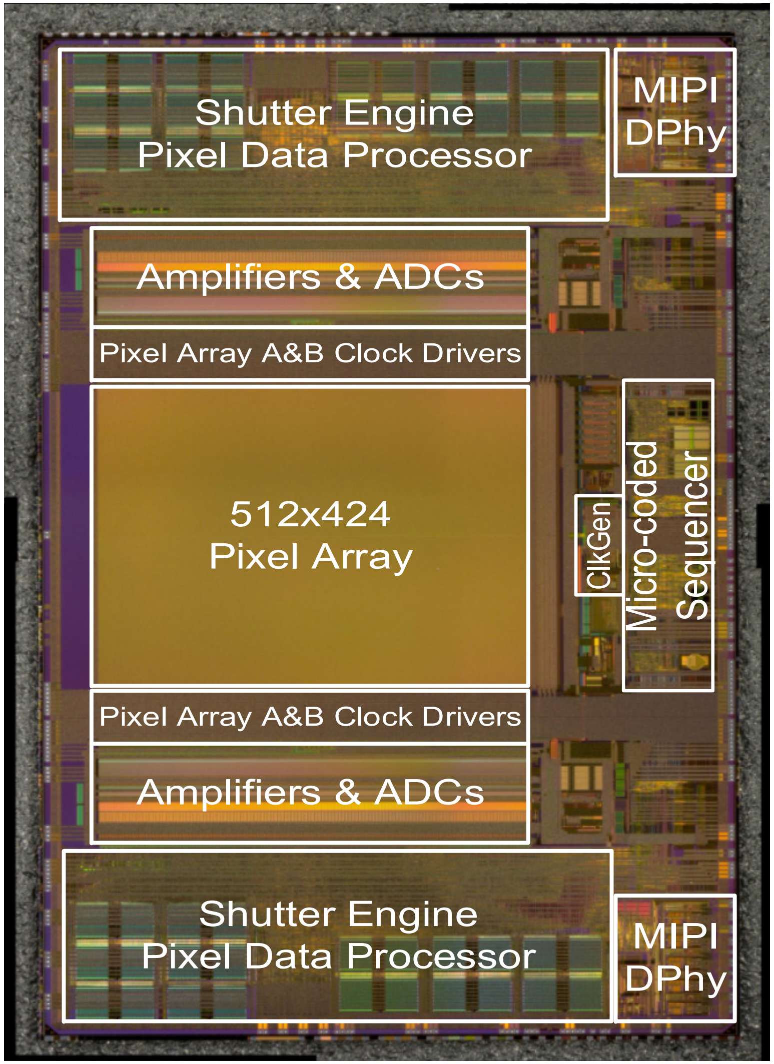
- Surface Plot
- Avg. 100 frames

- 30fps
- Room lighting
- Active IR



- Depth

Chip Micrograph



Features and Benefits

Feature	Benefit
512 x 424 Depth Pixels	Detect small distant objects in a large FOV
130MHz Modulation Frequency	Low depth jitter
Phase and Amplitude Detection	Measures depth and active IR images
Multi-Shutter/Gain Operation	Each pixel selects independent shutter/gain for expanded dynamic range
Multi-Frequency Operation	Solves depth range/precision conflict
Multi-Phase (>2 per frequency)	High accuracy and robustness
Motion Blur Resistant	Fast game movement
2 GS/s 10-bit ADC	Enables multi-shutter/frequency/phase and low motion blur
Integrated Shutter Engine	CDS & multi-shutter computation for IO bandwidth reduction
Programmable Sequence Control	Flexible multi-shutter/frequency/phase operation

Chip Specifications

Parameter	Value
Process Technology	TSMC 0.13μm 1P5M
Pixel Pitch	10μm x 10μm
Pixel Array	512 x 424
Chip size	8.2mm x 14.2mm
System Dynamic Range	>68dB
Modulation Contrast	68% @860nm @50MHz
Modulation Frequency	10~130MHz
FOV	70 (H) x 60 (V) degrees
Depth Uncertainty	<0.5% of range
Distance Range	0.8~4.2m

Parameter	Value
Operating Wavelength	860nm
Frame Rate	max 60fps (typical 30fps)
ADC	2GS/s
Effective Fill Factor	60%
Reflectivity	15%~95%
Chip Power	2.1W
Responsivity @860nm	0.144 A/W
Readout Noise	320μV differential
F#	1.07
ADC Resolution	10 bits

State of the art TOF Chip Comparison

Parameter	Unit	R. J. Walker, et al., 2011	D. Stoppa, et al., 2011	S.-J. Kim, et al., 2012	C. Niclass, et al., 2012	C. Niclass, et al., 2013	**This Work**
Depth image resolution	pixels	128x96	80x60	480x270	256x64	202x96	**512x424**
CMOS Technology	-	0.13μm imaging	0.18μm imaging	0.11μm imaging	0.18μm HV	0.18μm HV	**0.13μm**
Pixel fill factor	%	3.2	24	34.5	13.9	70	**60***
Illumination wavelength	nm	850	850	850	870	870	**860**
Illumination rep./frequency	MHz	3.33	20	20	0.3	0.133	**72 avg**
Field of view (HxV)	deg.	40x40	7.6x5.7	24x14	45x11	55x9	**70x60**
Frame Rate	fps	20	5	11	10	10	**30**
Target reflectivity	-	white	white	white	white	9%	**15%**

* With microlens

Summary

- State of the art TOF chip for indoor applications
- Large operating ROI (0.8~4.2m with 70° x 60° FOV)
- 512 x 424 depth measurement pixels
- 68dB dynamic range (multi gain/shutter)
- 68% modulation efficiency at 50Mhz (860nm)
- 130MHz maximum modulation frequency
- Multi-frequency operation
- 2GS/s ADC